ZENITH | data systems

INTERFACE BOARD

Model Z-89-67

595-2697

ZENITH DATA SYSTEMS
SAINT JOSEPH, MICHIGAN 49085

TABLE OF CONTENTS

INTRODUCTION

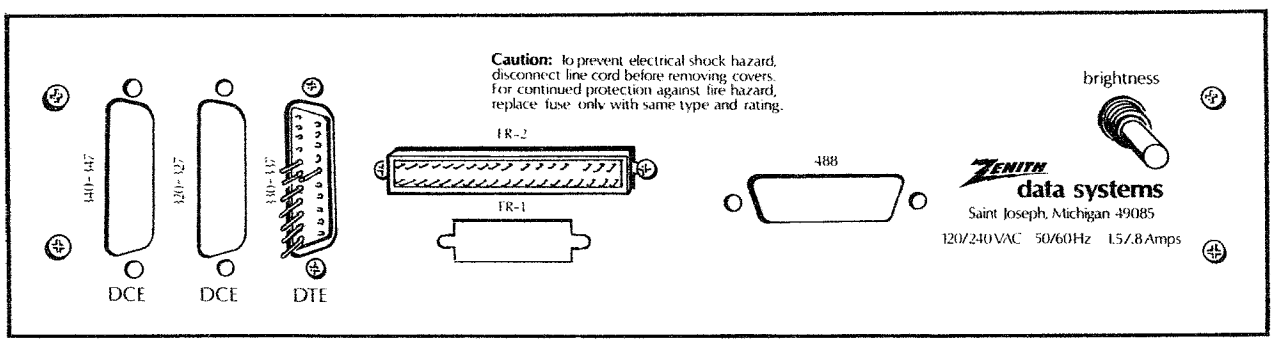
The Z-89-67 Interface Board connects the Z-67 Winchester Disk System to either a Z-89 or H-89 All-in-One Computer.

This Interface Board allows the Computer to:

- Communicate data to and receive data from the Disk Drive unit.
- Control the Disk Drive unit.
- Obtain status information about the Disk Drive.
- Read the DIP switches on the Interface Board to indicate equipment configuration.

The Interface operates under HDOS version 3.0 and later, CP/M* version 2.2.03 and later, and any other suitable software.

NOTE: If your Computer does not have a backplate like the one shown below, with provisions for a connector at FR-2, then you must also install the Z-89-6 Backplate Modification Kit before you install this product.



PICTORIAL 1

*Trademark of Digital Research, Inc.

HOST COMPUTER REQUIREMENTS

FIRMWARE

To run your system with a Z-89-67 Interface Board and the Z-67 Winchester Disk Drive installed, the following Read-Only Memory (ROM) chips must be installed (see "Initial Set-Up" for instructions):

1. Boot ROM MTR-90 (part number 444-84) at location U518 (supplied).

2. Secondary address decoder (part number 444-83) at location U516 (supplied).

3. I/O decoder (part number 444-61) at location U550 (supplied).

REAR PANEL AND CONNECTING CABLES

Newer computers have connectors FR-1 and FR-2 located on the back panel (see Pictorial 1). If your machine does not have these connectors, order Modification Kit Z-89-6.

DIP SWITCH SETTINGS

The CPU switch settings are detailed in the "Initial Setup" section.

COMPATIBILITY WITH OTHER INTERFACES

The Interface Board is fully compatible with them.

- H-88-1 single-density, 5-inch, hard-sectored controller.
- Z-89-37 double-density, 5-inch, soft-sectored controller.
- H-88-3 and HA-88-3 Serial Interfaces.
- Z-89-11 Multi-Format Interface.

The Interface Board is not compatible with the H-88-5 Cassette Interface.

It is possible to use the Interface with the Z-47 Dual 8-Inch Floppy Drives, but we do not recommend it.

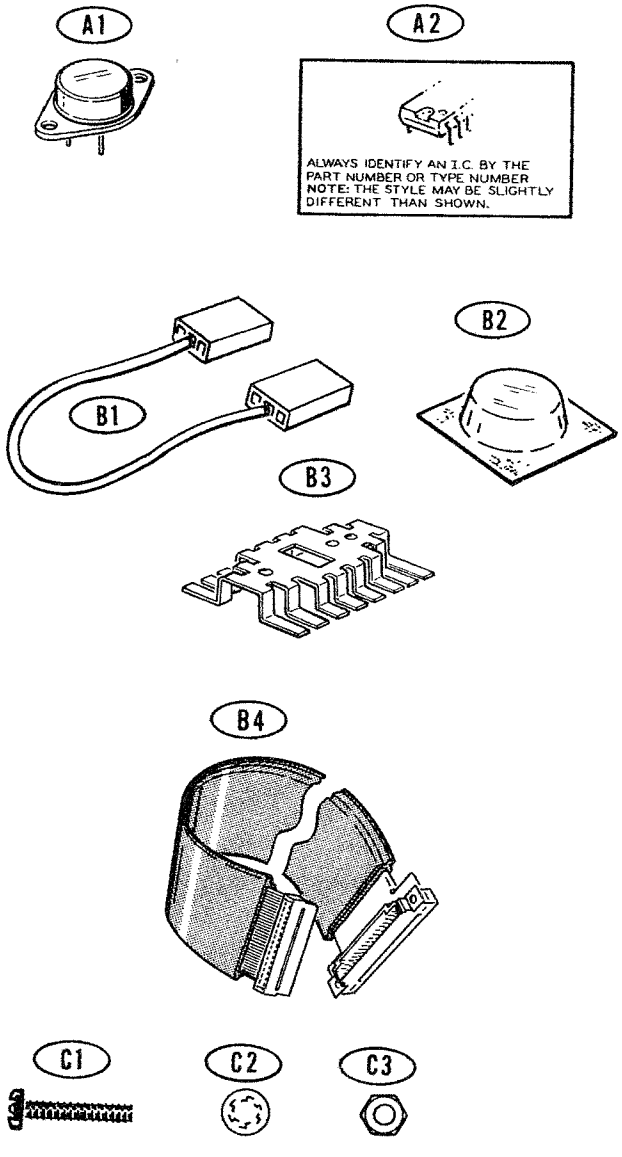
INITIAL SETUP

PARTS LIST

Check the parts you received against this Parts List and the Parts Pictorial. Any part that is packed in an individual envelope with a part number on it should not be removed from its envelope until it is called for in a step. Do not discard any packing materials until all parts are accounted for.

To order a replacement part, always include the Part Number.

KEY No.	HEATH Part No.	QTY.	DESCRIPTION	CIRCUIT Comp. No.
A1	442-651	1	5 volt regulator	U101
A2	444-61	1	ROM	U550
A2	444-83	1	PROM	U516
A2	444-84	1	PROM	U518
B1	134-1159	1	3" wire with connectors	
B2	352-31	1	Thermal compound	
B3	215-658	3	Heat sinks	
B4	134-1219	1	Ribbon cable	
C1	250-1319	2	#4-40 × 5/8" screw	
C2	254-9	2	#4 lockwasher	
C3	252-2	2	#4-40 nut	
		1	Operation Manual (see page 1 for part number)	
	595-2696	1	MTR-90 manual	
		1	Warranty	
		1	Service Center list	
		1	Registration Card	



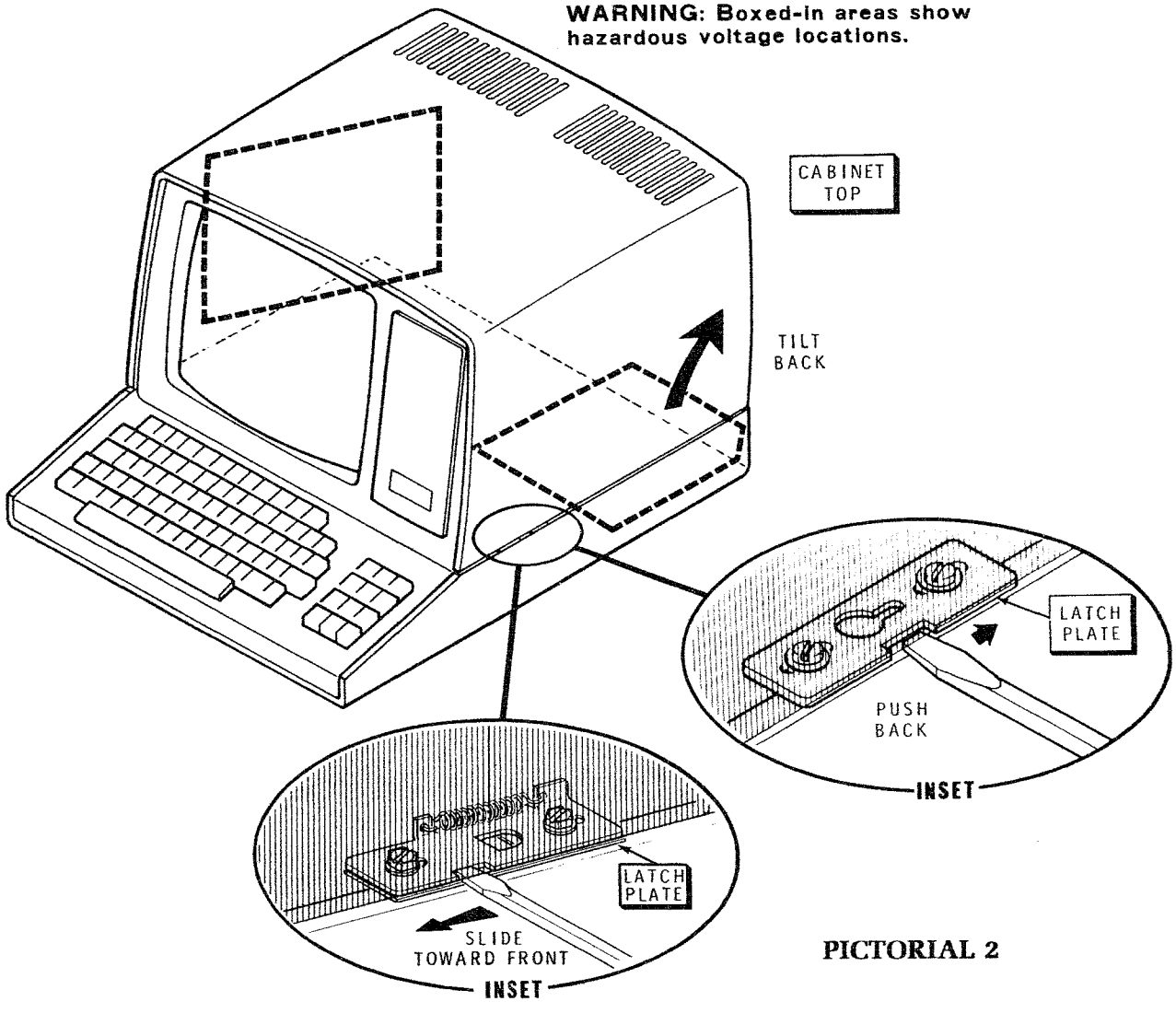
( ) Before you prepare the Interface Board for use, inspect it carefully. If it is damaged, return it. Pack it in at least four inches of insulating material.

PREPARATION FOR USE

COMPUTER TOP REMOVAL

- Turn the Computer off and unplug the line cord.
- Refer to the inset drawing on Pictorial 2 insert the blade of a small screwdriver into the notch in the latch plate, and then slide the latch plate as shown in the inset drawings.
- Likewise, open the latch plate on the other side of the cabinet top.
- Carefully tilt the cabinet top back. NOTE: The hinges are designed so you can easily remove the top once you have opened it completely.
- Unplug the fan.

Reverse this procedure to close and lock the cabinet top back on the Computer when you are done.



PICTORIAL 2

CPU REMOVAL

Refer to Pictorial 3 (Illustration Booklet, Page 1) for the following steps.

( ) Remove the two screws that hold the CPU logic circuit board in place.

( ) Disconnect the cables from the circuit board, lift the circuit board up out of the Computer, and set the board aside temporarily. (If a serial I/O board is installed, also unplug its cables.)

POWER SUPPLY REMOVAL

( ) Refer to Pictorial 4 (Illustration Booklet, Page 2) and examine your Computer to see if there are heat sinks at U101, U102, and U103. If heat sinks are present, and U101 is a type 78H05 or 78-T05 (#442-651) IC, you may proceed to "CPU Installation" on Page 8. Otherwise, perform the following steps.

Refer to Pictorial 5 (Illustration Booklet, Page 3) for the following steps.

( ) Disconnect the four cables from the power supply circuit board. Then remove the four corner screws and set the circuit board aside.

( ) Remove the four hex spacers and lift the power supply heat sink out of the Computer. Do not disconnect any wires that are soldered to the heat sink assembly.

Refer to Pictorial 4 (Illustration Booklet, Page 2) and Detail 4A for the following steps.

( ) Remove the two screws that hold IC socket U101. Then remove and discard the IC, and set the screws aside.

WARNING: You will be using Dow Corning 340 thermal compound in the following steps. Although this compound is not caustic, it may cause temporary discomfort if it gets into your eyes. If this happens, rinse your eyes with warm water. If the compound gets on your clothing, it may require professional cleaning, so handle the compound carefully. This compound contains zinc oxides, SiO_2 and slight traces of CO_2.

( ) Locate the thermal compound pod and make a small slit in one side.

( ) Spread a small amount of thermal compound onto the UA**78H05**SC or MC**78T05** integrated circuit (#442-651). Squeeze the pod to remove the compound.

( ) Spread a small amount of thermal compound on the back of the regulator heat sink.

( ) U101: Refer to Detail 4A and note the wide space of the IC. Install the IC in the socket and the regulator heat sink at U101. Be sure the socket is properly seated in its mounting holes in the heat sink, and then install the two screws you removed earlier.

NOTE: If your Computer already has heat sinks at U102 and U103, proceed to "Power Supply Installation." If your Computer does not have heat sinks at these locations, proceed with the following steps.

( ) Remount the IC regulator at U102. Use a regulator heat sink and thermal compound as before.

( ) Remount the IC regulator at U103. Use a regulator heat sink and thermal compound as before.

POWER SUPPLY INSTALLATION

Again refer to Pictorial 5 (Illustration Booklet, Page 3) for the following steps.

( ) Remount the power supply heat sink with the four 6-32 hex spacers you removed earlier.

( ) Remount the power supply circuit board with the four 6-32 × 1/4" screws that you removed earlier. NOTE: If your unit had a lockwasher installed at A, you must reinstall it at A as shown.

If you have a voltmeter, make the following tests. Otherwise, proceed to "CPU Installation."

( ) Connect the common voltmeter lead to the heat sink as shown on Pictorial 4.

NOTE: If you do not obtain the proper results in the following steps, immediately unplug the line cord and correct the problem before you proceed.

( ) Plug in the line cord and turn on the Computer.

( ) Measure TP1. The voltage should be +4.5 to +5.5 volts DC.

( ) Measure TP2. The voltage should be +4.5 to +5.5 volts DC.

( ) Measure TP3. The voltage should be +10.8 to +13.2 volts DC.

( ) Turn off the Computer and unplug the line cord. Then disconnect the voltmeter and set it aside.

( ) Reconnect the four cable plugs to the power supply circuit board.

CPU INSTALLATION

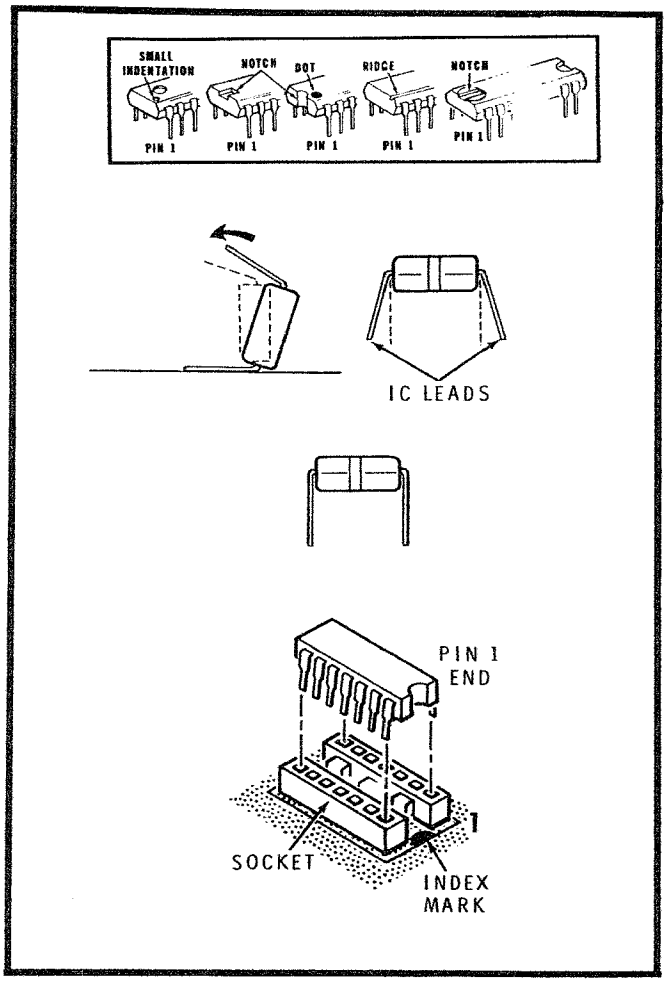
Again refer to Pictorial 3 for the following steps.

NOTE: The following steps tell you to remove some IC's. Some of these devices are reusable 2716 EPROM's. Keep them if you like, or discard them.

( ) U516: Refer to inset drawing #1 on Pictorial 3 and check to see if the IC at U516 is a 443-83 (it will be marked). If it isn't, remove it. Then refer to Detail 3A and install the 74**S188** IC (#444-83) at U516. This part is a programmed PROM.

( ) U518: Check U518 to see if it is a 444-84. If it isn't, remove it and install the 2732 IC (#444-84). (If your Computer has the 16K adapter circuit board installed, temporarily remove it if necessary.) This part is a programmed PROM.

( ) U550: Check to see if U550 is a 444-61. If it isn't, remove the IC. Then install the I/O decoder ROM IC (#444-61) at U550.



Detail 3A

Refer to Pictorial 6 (Illustration Booklet, Page 4) for the following steps.

( ) On the left side of the CPU circuit board is a row of four programming plugs as shown in the Pictorial. Remove and set aside the top plug (it will not be used). Then reposition the middle two plugs from 0 to 1. The bottom plug will not be changed.

( ) Plug one end of the 3" wire with connectors onto the top plug near U518. (Be sure the connector plugs onto all three pins of the plug.) Plug the other end of the wire onto plug P508. Be sure the center hole of the connector is connected to pin 14 of the plug. (The plug is numbered from top to bottom.)

Board. How you install yours depends on what equipment you already have. If you have:

1. **A Z-89-37 Double Density Controller**, you must install your Interface Board as shown in Pictorial 7 (Illustration Booklet, Page 5). Switch SW501 on the CPU Board must be set as shown in inset drawing #1. The jumpers on the Interface Board must be set as shown in inset drawing #2.

2. **An H-88-1 Disk Controller**, you must install your Z-89-67 Interface Board as shown in Pictorial 8 (Illustration Booklet, Page 5). Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

3. **A Z-89-47 Interface Board**, you must install your Z-89-67 Interface Board as shown in Pictorial 9 (Illustration Booklet, Page 6). Set switch SW501 as shown in inset drawing #1, and the jumpers as shown in inset drawing #2.

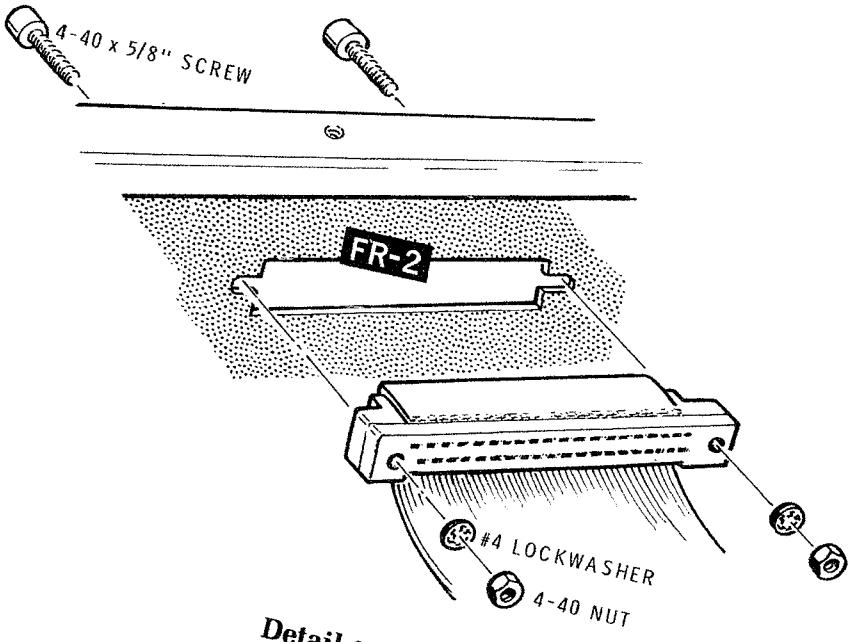
4. **None of the Above**, Board as shown in P Booklet, Page 6). S shown in inset drawin as shown in inset draw

You may set the DIP switches on in any position when you are usin

( ) Connect the Interface Board t panel with cable 134-1219, as 10A, using two #4-40 × 5/8" lockwashers, and two 4-40 nu have FR-2 on the rear panel of order Modification Kit Z-89-6 fr or from Zenith Data Systems. M on the cable is pointed up.

( ) Replace the accessory mounting br

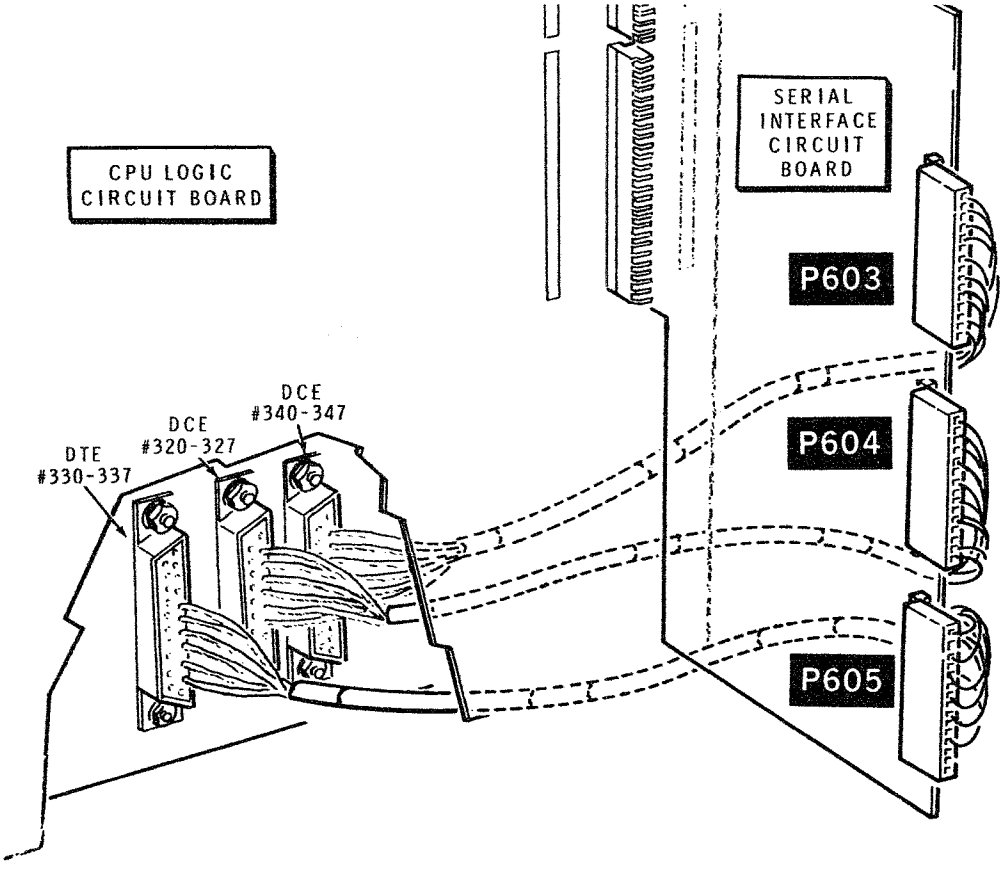
( ) Connect the Z-67 Winchester Disk D FR-2 with the Winchester's 40-pi cable, as explained in the Winchester



Detail 10A

( ) Refer to Pictorials 3 and 11 and reinstall the CPU logic circuit board. Secure it in place with its two screws and reconnect the cables as shown. (Be sure to reconnect P513 in the bottom right-hand corner of the CPU board.)

( ) Replace the cabinet top.



PICTORIAL 11

SOFTWARE ACCESS

This section provides programmers with software information to access the Z-89-67 Interface and Z-67 Winchester Disk Drive.

SOFTWARE THEORY OF OPERATION

A command is executed in the following manner:

1. The device driver builds a Command Descriptor Block (CDB) in system memory.

2. The driver then writes the address of the first byte of the CDB into the Command I/O Pointer Block (CIOPB) of the command driver routine.

3. The Data Address (DAD) is also set up if a data transfer is required. Commands requiring data transfers are READ, WRITE, REQUEST SENSE, and REQUEST SYNDROME.

4. The driver now performs a GETCON routine that determines if the controller is busy. If it is not busy, the GETCON routine asserts the SELECT line until the controller responds with a busy.

5. When the controller responds to the Interface Board by asserting BUSY, the driver shifts to the OUTCON routine. In response to the REQuest bit in the BSTAT, the driver passes the command a byte at a time to the controller.

6. The controller verifies that the command is correct and begins the command execution phase. At this time, the data is tranferred to or from the Interface Board and into or out of the main memory. The data transfer may be initiated by an interrupt on receipt of the first REQ after the Interrupt enable bit is set in the command register.

7. After the data transfer is completed, the controller enters the command completion phase. The controller sends a one-byte status to the Interface Board, indicating whether or not an error occurred during command execution. This is handled by the CMPSTAT routine. Finally, the controller sends the message byte (of zeros) and the operation is complete.

8. At this time, the controller enters the idle mode, awaiting another command. If the controller encountered an error, the CMPSTAT routine returns with it in the Y register. It is the responsibility of the device driver to issue REQUEST SENSE command to request any detailed information about the error.

INTERFACE REGISTER DEFINITION

The registers on the Interface Board are listed below. The address given assumes that the Board is installed at P504, P510 (addresses 170-173 octal). If the Board is installed at P506, P512, add four to the address given.

HEX Address	Register
78 hex, 170 octal	Data In/Out Register (DAR)
79 hex, 171 octal	Control Register — Write Only (CNR) Status Register — Read Only (BSTAT)
7A hex, 172 octal	DIP Switches

The bit definition for each register is described below.

Control Register (CNR)	Output Address (79 hex, 171 octal)
Bit 7	Not Used
Bit 6	SEL — Assert Select and Data Bit 0 used to access a controller.
Bit 5	Inten — Interrupt Enable — Causes interrupt if REQ present.
Bit 4	Reset
Bit 3	Not Used
Bit 2	Not Used
Bit 1	Data Enable
Bit 0	Not Used

Bus Status	Input Address (79 hex, 171 octal)
Bit 7	REQ — Indicates the controller in the Z-67 either requests data or has data for the Interface Board.
Bit 6	IN/OUT (referenced to controller) — Low indicates data to Interface Board. High indicates data to controller.
Bit 5	MSG — Indicates last byte in data or command string.
Bit 4	COM/DTA — Is high when a command is being sent to the controller, and is low when data is being sent.
Bit 3	BUSY — Indicates status of busy signal.
Bit 2	PARITY ERROR — Indicates bad parity.
Bit 1	INT IN PROGRESS — Verifies that interrupt has been activated. Reading status port resets interrupt.
Bit 0	ACK — Acknowledges request for data.

INTERFACE BOARD BUS PIN ASSIGNMENT

The Interface Board is connected to the Z-67 controller through a 40-pin connector.

The pin assignments are as follows:

Signal	Pin Number
DATA0	2
DATA1	4
DATA2	6
DATA3	8
DATA4	10
DATA5	12
DATA6	14
DATA7	16
PARITY	18
———	20 (spare)
GROUND	21
———	22 (key)
GROUND	23
———	24 (spare)
BUSY	26
ACK	28
RST	30
MSG	32
SEL	34
C/D	36
REQ	38
I/O	40

NOTE: All signals are active low and all odd pins are connected to ground. The signal lines are terminated with 220 Ω to 5 V and 330 Ω to ground.

COMMANDS/PROGRAMMING

An I/O request to the Z-67 disk controller is performed by passing a command descriptor block (CDR) to the Z-67 Winchester Drive. The first byte of a CDR is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, and number of blocks to transfer. The controller performs an implied seek and verify when it is commanded to access a block.

Please refer to your Z-67 Manual for more specific information about the Z-67 disk controller.

COMMAND FORMAT

Commands Requiring 6 Bytes:

Command Byte 0	XXXX
Command Byte 1	XXXX+1
Command Byte 2	XXXX+2
Command Byte 3	XXXX+3
Command Byte 4	XXXX+4
Command Byte 5	XXXX+5

XXXX is the address that is stored in CIOPB.

Commands requiring 10 Bytes:

Command Byte 0	XXXX
Command Byte 1	XXXX+1
Command Byte 2	XXXX+2
Command Byte 3	XXXX+3
Command Byte 4	XXXX+4
Command Byte 5	XXXX+5
Command Byte 6	XXXX+6
Command Byte 7	XXXX+7
Command Byte 8	XXXX+8
Command Byte 9	XXXX+9

XXXX is the address that is stored in CIOPB.

REQUEST SYNDROME COMMAND

The REQUEST SYNDROME command returns two bytes of information. The data returned for the REQUEST SYNDROME command is listed as follows:

Data Byte 0	XXXX
Data Byte 1	XXXX+1

XXXX is the address that is stored in the DMA location.

DRIVE AND CONTROLLER SENSE INFORMATION

Upon execution of the REQUEST SENSE command, the controller returns four bytes of information in the following format (refer to the Z-67 Manual for detailed information about these bytes):

Data Byte 0	XXXX
Data Byte 1	XXXX+1
Data Byte 2	XXXX+2
Data Byte 3	XXXX+3

XXXX is the address that is stored in the DMA location.

NOTE: Data that is received from the controller as well as data that is sent to the controller is transferred in the above order.

OTHER COMMANDS

The Interface Board uses programmed I/O, taking advantage of the fact that the Z-67 Drive has a built-in sector buffer. The control lines of the Interface bus are available to the CPU through the Bus Status and Control registers. Data and commands are transmitted through the Interface bus by a simple handshake procedure as outlined in this and the Z-67 Manual.

The following types of commands are available to the user:

STATUS Sends drive status from controller to Interface Board.

```
TEST DRIVE READY
REQUEST SENSE
REQUEST SYNDROME
```

MOTION CONTROL Moves heads without R/W operation.

```
SEEK
RECALIBRATE
```

R/W Read/Write Operations.

```
READ
WRITE
COPY
```

FORMAT Formats drive or tracks with specified standard format.

```
FORMAT TRACK
FORMAT BAD SECTOR
FORMAT DRIVE
```

COMMAND SEQUENCE

Status Commands:

```
GET CONTROLLER
SEND COMMANDS (to controller)
READ STATUS DATA
READ COMPLETION STATUS
```

Motion Control:

```
GET CONTROLLER
SEND COMMANDS (to controller)
LOAD DATA
COMPLETION STATUS
```

Read/Write Sectors:

```
GET CONTROLLER
SEND COMMANDS (to controller)
WAIT FOR REQ
READ/WRITE DATA
READ COMPLETION STATUS
```

Copy:

```
GET CONTROLLER
SEND COMMANDS (to controller)
READ COMPLETION STATUS
```

PROGRAMMING

Some definitions (NOTE: Addresses given assume installation at P504, P510. For installation at P506/P512, add four to all addresses):

```
BASE equals Base I/O Address (78 Hex, 170 Octal).
DATAIN equals BASE.
DATAOUT equals BASE.
BCON equals BASE + 1 and is Bus Control.
BSTAT equals BASE + 1 and is Bus Status.
CIOPB is Command Address.
DMA is Data Address
```

Some sample assembly programs:

```
GET CONTROLLER

GETCON:  IN BSTAT        ;input from status port
         ANI 08H         ;select bit 3 (busy)
         JNZ GETCON      ;if busy wait in getcon loop
         MVI A,40H       ;get ready to assert SEL and DATAO
         OUT BCON        ;to get attention of controller
CBUSY:   IN BSTAT        ;input from bus status
         ANI 08H         ;again look at busy
         JZ CBUSY        ;arrived at controller attention else loop
         MVI A,02H       ;get ready to allow data enable
         OUT BCON        ;done
         RET             ;return from get controller routine

OUTPUT COMMANDS

OUTCOM:  LHLD CIOPB      ;load pointer to command queue
COMREQ:  IN BSTAT        ;input from bus status
         MOV C,A         ;store in C
         ORA A           ;set flags
         JP COMREQ       ;wait for REQ
         ANI 10H         ;check for command/data
         RZ              ;return when data is requested
         MOV A,C         ;also see if controller switched direction
         ANI 40H
         RZ              ;return if controller sends data
         MOV A,M         ;move commands from queue to accumulator
         OUT DATAOUT     ;write commands to controller
         INX H           ;increment pointer
         JMP COMREQ      ;loop as long as commands are requested from
                          controller
```

SEND DATA TO Z-67 WINCHESTER DRIVE (a WRITE operation)

```
WRITE:   LHLD DMA        ;load pointer to data
DAREQ:   IN BSTAT        ;input from bus status
         MOV C,A         ;store
         ANI 80H         ;set flags
         JZ DAREQ        ;wait for REQ
         ANI 10H         ;check for COM
         JNZ CMPSTAT     ;on receipt of command completion status is
                          present
         MOV A,M         ;move data into accumulator
         OUT DATAOUT     ;output to controller
         INX H           ;increment pointer
         JMP DAREQ       ;go back for another byte
CMPSTAT: IN DATAIN       ;input completion status
         MOV C,A         ;place in C for further use
LREQ:    IN BSTAT        ;looking for last REQ
         MOV B,A         ;save for checking
         ANI 80H         ;check for REQ
         JZ LREQ         ;loop until found
         IN DATAIN       ;input last byte
         ORA A           ;see if last byte is non-zero
         JNZ BADBYTE     ;if last byte is non-zero
         MOV A,C         ;now check completion status
         ORA A           ;to see if it is zero
         JNZ BADSTAT     ;if not zero
         MOV A,B         ;now check last bus status
         ANI 01H         ;for parity error
         JNZ BADPAR      ;high is bad parity
         XRA A           ;zero accumulator
         RET             ;return
```

READ DATA FROM Z-67 WINCHESTER

```
READ:    LHLD DMA        ;load data pointer
RDREQ:   IN BSTAT        ;input bus status
         MOV C,A         ;store for further checking
         ANI 80H         ;look for REQ
         JZ RDREQ        ;else loop
         MOV A,C
         ANI 10H         ;check for COM
         JNZ CMPSTAT     ;if COM present must be completion status
         IN DATAIN       ;input data from controller
         MOV M,A         ;move data to pointer
         INX H           ;increment pointer
         JMP RDREQ
```

CIRCUIT DESCRIPTION

INTRODUCTION

Refer to Pictorial 12 (Illustration Booklet, Page 7), a Block Diagram of the Z-89-67 Interface Board, while you read the following description.

The Interface has five functions:

1. Input data buffering
2. Output data buffering
3. Status buffering
4. Parity generation and checking
5. Control buffering

Data is read and written through the bidirectional data buffer, the read/write data latches, and the data transceivers. The data transceivers communicate with the Z-67 transition and controller boards. The data transmission lines have low-pass filters installed (L1-L8) to attenuate high frequency noise.

Read/Write control, status buffering, and resets are accomplished by means of the control signal decoder, interrupt logic, status buffer, control latch, and reset/acknowledge latch and generator. These circuits communicate with the Z-67 Winchester Disk Drive through the control line drive and receive buffers. The control transmission lines are filtered in the same way as the data transmission lines (by L9-L17).

Parity generation and checking is accomplished by the data parity generator/checker. Odd parity is generated. When a write is performed, the Z-89-67 Interface Board sends a parity bit to the Z-67 Drive along with the data word. When a read is performed, the Interface Board checks the parity bit sent from the Winchester Disk Drive to determine if the data is correct.

The positions of the DIP switches are read through the DIP switch buffer and data bus.

Please refer to the Schematic (fold-in) as you read the following descriptions.

U1 Bidirectional Data Buffer — U1 buffer allows data to pass either as input from or output to the computer, depending on the condition of the read line and board select line. In other words, if the read and board select lines are enabled, U1 will admit only output to the Computer. If the READ line is not enabled, but the board select line is, U1 will admit only input from the Computer.

U2 Read Data DIP Switch Buffer — U2 buffers the DIP switch condition on the read cycle only. It is enabled by the RD SWITCH (read switch) line.

U3 NAND Gates — U3 is a set of four NAND gates that qualify various control signals on the board.

U4 Read/Write Control Decoders — U4 consists of U4A, the read address decoder, and U4B, the write address decoder. These two circuits decode signals from the computer to the Interface Board. All control signals except reset are decoded by U4. The reset signal is handled by the reset generator and control latch (U15 and U20A).

U5 Buffer Inverter — U5 performs the double function of inverting and isolating signals. U5 consists of four inverters, A, B, C, and D. (There are two others, but they are not used).

U6 and U7 NAND Gates — U6 NAND's signals that must be present together for an operation to occur. (U6C, U6D, and U7D are not used.)

U8 AND Gates — U8 AND's signals that must be present together for an operation to occur.

U9 Parity and Acknowledge Flip Flops — U9A latches the parity signal from the parity checker (U11) and sends it to the status buffer (U14), through which the condition of legal parity may be checked by the Computer.

U9B latches the request signal from the Winchester Disk Drive and sends back an acknowledge, unless the acknowledge hold signal from the control latch (U15) is active.

U10 Interrupt Flip Flops — U10, in conjunction with U6A and U8D, determines if a request interrupt from the Winchester Drive may occur.

U11 Parity Generator/Checker — U11 generates a parity bit on a write cycle and checks parity on a read cycle. It checks for even or odd parity, depending on whether jumper J4A or J4B is set. Normally, J4B is set, producing odd parity.

U12 Read Latch — U12 latches data signals from the transceivers U16 and U17. The latched signals are sent to the bidirectional buffer (U1) on the internal data bus for transmission to the Computer during a RD DATA cycle.

U13 Write Latch j8 U13 latches data from the internal data bus and sends them to the transceivers (U16 and U17).

U14 Status Buffers — U14 buffers the status lines from the Winchester Drive to the internal data bus.

U15 Control Latch — U15 latches the select control signals from the Computer to the Winchester Drive. U15 also latches the acknowledge hold and request interrupt enable control signals from the Computer to the rest of the Interface Board.

U16 and U17 Transceivers — U16 and U17 are line drivers/receivers that accept write data from U13 and read data from the Z-67 transmission cable.

U18 Open Collector Buffer — U18 buffers control signals acknowledge, reset, select, and data bit 0.

U19 and U21 Divide-by-Eight Counters — U19 and U21 divide the computer's system clock signal to help U20 generate the reset signal.

U20 Reset Flip Flop — U20 generates a reset under software control. The reset is strobed by the divide-by-eight counters to the Computer. (U20B is not used.)

READ MECHANISM

When the Computer is turned on, it sends a reset signal to the Z-89-67 Interface Board. This reset clears whatever state the board happens to be in. The reset signal comes in at pin 15 of P2, is buffered by U5B and U5C, and resets control latch U15, interrupt logic U10B and U10A, and divide-by-eight counter U21.

When the Computer wants to read data from the Winchester Disk Drive, it sends control signals to the disk drives through U1, the bidirectional buffer (which is normally set to allow input from the Computer rather than input from the drives). The control signals travel over the internal data bus to control latch U15, which passes the SEL (drive select) control signal to the drives through buffer U18 and P3.

When the proper drive receives the select signal, it responds with a BUSY signal, which the Computer reads from status buffer U14 by changing the direction of buffer U1 with a BRD signal. The Computer then removes the select signal from the line by resetting Control Latch U15. The Winchester Drive responds with a REQ, or request, signal. This signal is ANDed with a REQ INT EN (request interrupt enable) at U8D to produce an interrupt to the Computer via buffer U6A. (The REQ INT EN comes from the U15 control latch).

The other control signals are ACK Hold (acknowledge hold) and REQ INT EN (request-interrupt enable). The first is used to prevent the Z-67 controller from assert-

ing a REQ to the Interface Board, while the latter allows the drives to interrupt the computer (however, in the standard system software, interrupts are not used, so REQ INT EN is ignored).

Another control signal that comes off of the data bus is the software controllable reset signal (data bit 4). This data bit is routed directly to reset latch U20A. From there, the reset is strobed by counter U21 to buffer U18C, where it is passed on to the drives.

To continue the read process after receiving an interrupt, the computer sends either an I/O FLPY signal to pin 11 of P2 or an I/O DSK signal to pin 12 of P2 on the Interface Board. (If I/O FLPY is used, the Interface Board is mounted in the right I/O port, that is, P512 and P506 on the CPU board. Also, pin 2 of U5A must be jumpered to pin 2 of U3A, and pin 11 of P2 must be jumpered to pin 1 of U3A. If I/O DSK is used, the Board is mounted in either of the remaining I/O ports, P511 and P505 or P510 and P504, on the CPU board, and pin 1 of U5A must be jumpered to pin 2 of U3A, while pin 12 of P2 must be jumpered to pn 1 of U3A.) One of these signals is ANDed at U3C with BA2 on pin 5 of P2.

The resulting BRD SEL (board select) signal, routed to U1, U3A, and U3B, means that the Interface Board is enabled to interpret control signals from the computer. A BRD (buffered read) signal is also received at pin 6 of P2. BRD is ANDed at U3A with the BRD SEL signal from U3C. Depending on the address signals BA0 and BA1, the resulting signal activates either the RD DATA signal or the RD Switch signal at U4B (one of the Control Decoders). RD DATA causes data to be read from the appropriate disk drive, while RD Switch allows the DIP switch SW1 to be read.

RD Data enables the read latch U12. RD Data also sets the acknowledge flip flop U9B (through OR gate U8A), sending an acknowledgment signal to the disk drive (by means of buffer U18B). The acknowledgment tells the Z-67 Winchester Drive that the interrupt was received.

Data can now be transmitted from the Z-67 Winchester Disk Drive unit to the Z-89 Computer.

WRITE MECHANISM

When the Computer needs to write data to the Winchester Drive, it sends control signals to the disk drives through U1. The drives respond with the same handshaking procedure as before. However, instead of receiving a BRD at P2, a BWR is received by the Interface Board at pin 7 of P2.

The BWR (buffered write) is ANDed with the BRD SEL signal at U3B. The resulting signal activates the LD Data (load data) and LD CON (load control) lines from U4B.

LD DATA enables the write latch U13 and the acknowledge flip flop U9B (through OR gate U8A). The acknowledgment tells the Winchester that data will now be written onto the drive that was selected.

IN CASE OF DIFFICULTY

The Z-89-67 Interface Board was not designed to be user-serviceable. If it does not function properly, or if the Computer does not boot or read disks from the H-88-1 Controller, check the jumpers on the Board for the following settings:

Parity	Odd
BA2	/BA2 (depending on which I/O port was used)
I/O	DSK (depending on which I/O port was used)
RESET	32 μs
INT3	none
INT4	none
INT5	none

DIP switch settings are defined by your software system. Consult your operating system manual for proper switch settings. If your system does not read the DIP switch, then the switch may be left in any position.

Ensure that the correct ROM's and ROM jumpers are installed on the CPU board.

Make sure that the Interface Board is seated correctly on the CPU board and is not installed a pin or two off.

Ensure that the data cable to the Interface Board is connected and that pin 1 (the colored wire) is at the top.

If your Interface Board needs servicing:

- Call your local Zenith Data Systems Dealer,

or

- Call the nearest Authorized Zenith Data Systems Service Center (check the list accompanying this product or look in the yellow pages under "Data Processing Equipment"),

or

- Call the nearest Heathkit Customer Center,

or

- Call Zenith Data Systems, Customer Service Assistance, at

(312) 671-7550.

IMPORTANT: Be prepared to furnish the following information. It will be helpful in diagnosing and repairing your unit.

A. The problem you are having.

B. Name and model of your computer system.

C. Baud rate.

D. System configuration.

E. Any additional information that will help describe your system.

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
RESISTORS		
RP1-RP3	9-124	4700 Ω resistor pack
RP4-RP6	9-123	220 Ω/330 Ω resistor pack
CAPACITORS		
C1-C2	25-220	10 μF, 20 V tantalum
C3-C23	21-762	0.1 μF, 25 V ceramic
C24-40	21-757	22 pF, 50 V ceramic
INDUCTORS		
L1-L17	475-15	1.22 μH ferrite bead
INTEGRATED CIRCUITS		
See "Semiconductor Identification Chart"		
CABLE		
	134-1219	Ribbon cable

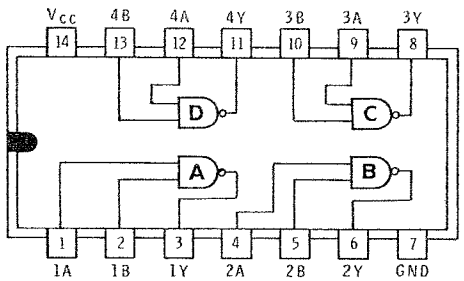
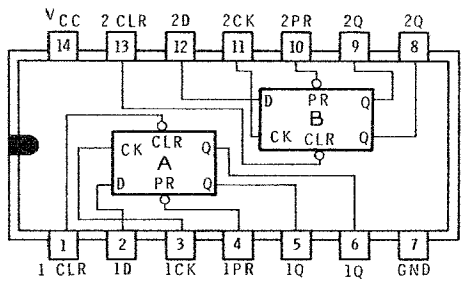
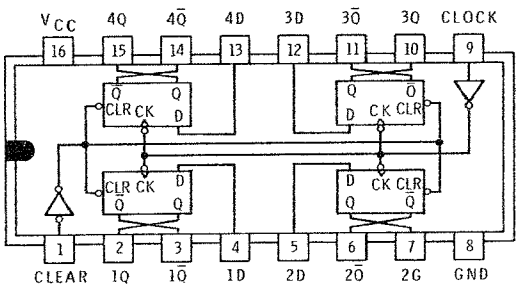
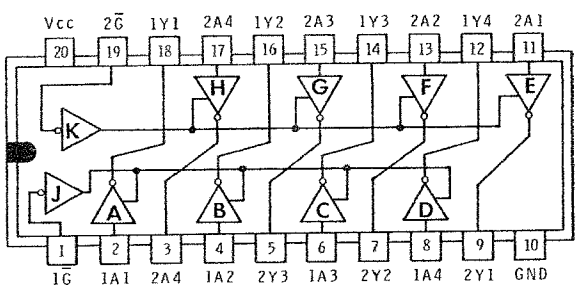
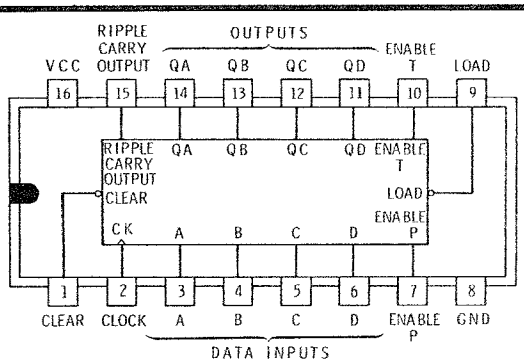
SEMICONDUCTOR IDENTIFICATION CHARTS

COMPONENT NUMBER INDEX

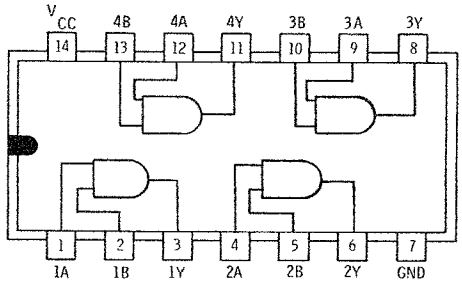
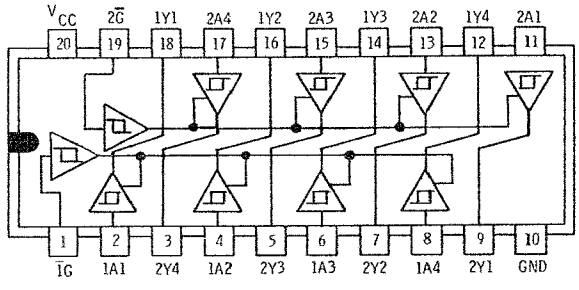
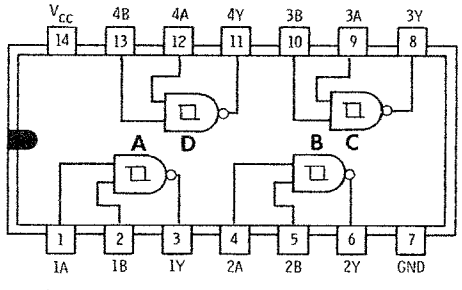
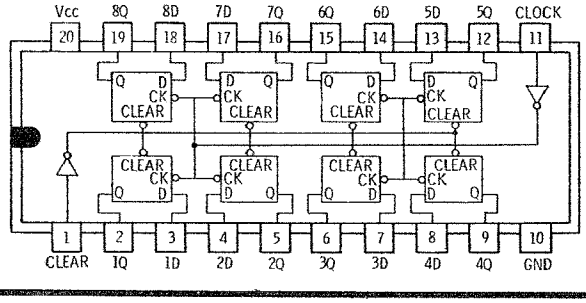
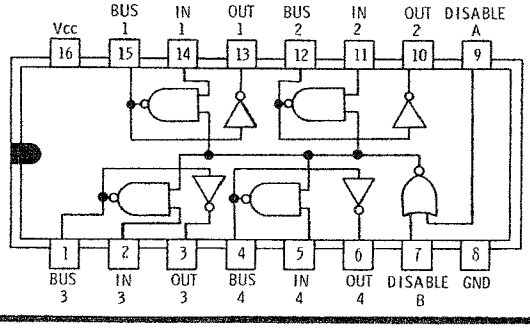
CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U1	443-885
U2	443-791
U3	443-875
U4	443-822
U5	443-872
U6	443-77
U7	443-792
U8	443-780
U9	443-730
U10	443-730
U11	443-1001
U12	443-863

CIRCUIT COMPONENT NUMBER	HEATH PART NUMBER
U13	443-805
U14	443-754
U15	443-752
U16	443-819
U17	443-819
U18	443-77
U19	443-757
U20	443-730
U21	443-757

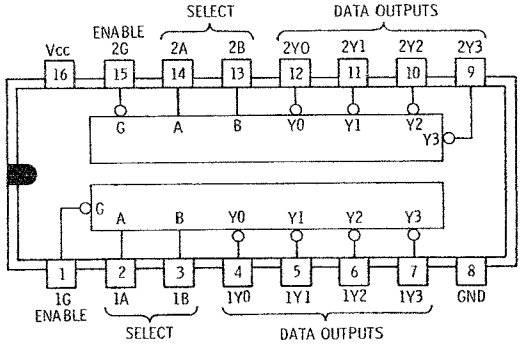
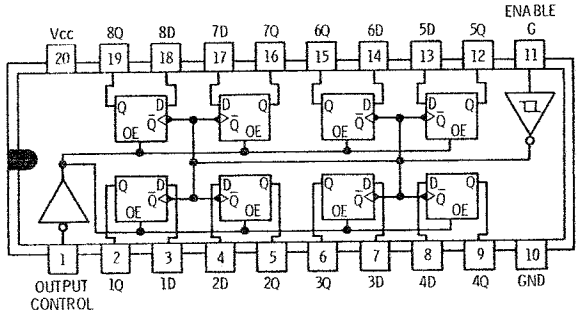
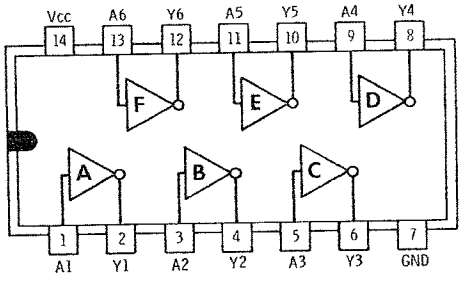
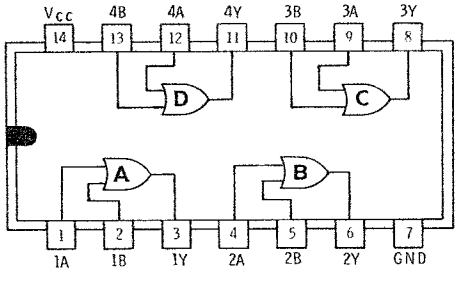
PART NUMBER INDEX

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-77	7438N	QUAD 2-INPUT NAND GATE (open collector)	
443-730	74LS74	DUAL D FLIP FLOP	
443-752	74LS175	QUAD LATCH	
443-754	74LS240	INVERTING OCTAL BUFFER 3 STATE	
443-757	74LS161	SYNCHRONOUS DIVIDE BY 16 COUNTER	

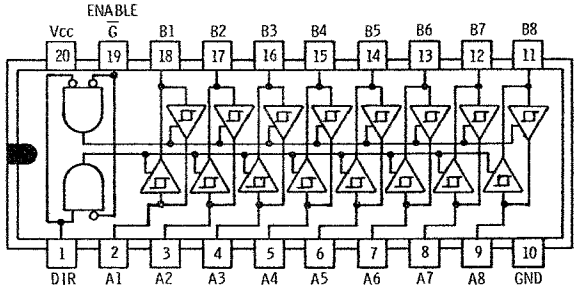
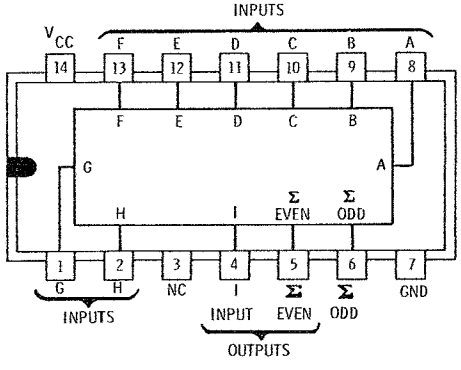
Part Number Index (Cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-780	74LS08	QUAD 2-INPUT AND GATE	
443-791	74LS244	NON-INVERTING OCTAL BUFFER 3 STATE	
443-792	74LS132	QUAD 2-INPUT SCHMITT TRIGGER	
443-805	74LS273	8 BIT LATCH	
443-819	DS8838	QUAD BUS TRANSCEIVER (OPEN COLLECTOR)	

Part Number Index (Cont'd.)

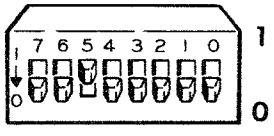
HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-822	74LS139	DECODER DUAL 2-4 LINE	
443-863	74LS374	8 BIT 3-STATE LATCH	
443-872	74LS14	HEX SCHMITT TRIGGER INVERTER	
443-875	74LS32	QUAD 2 INPUT OR GATE	

Part Number Index (Cont'd.)

HEATH PART NUMBER	MAY BE REPLACED WITH	DESCRIPTION	IDENTIFICATION
443-885	74LS245	NON-INVERTING, 3-STATE, OCTAL BUS TRANSCEIVER	
443-1001	74LS280	PARITY GENERATOR/CHECKER	
444-61*	NOT APPLICABLE	I/O DECODER	NOT APPLICABLE
444-83*	NOT APPLICABLE	STTL EPROM	NOT APPLICABLE
444-84*	NOT APPLICABLE	NMOS EPROM	NOT APPLICABLE

*Available only from Heath/Zenith.

APPENDIX



CPU DIP Switch SW501, located at the lower right of the Z-89/90 CPU Board, has eight sections (0 to 7) that may be set to either one or zero. These sections have the following functions:

SECTIONS	SETTINGS	SETTING DEFINITION	SECTION DEFINITION
1,0		00 — Hard-sectored 5.25-inch disk. 01 — H/Z-47 eight-inch floppy. 10 — Z-67 Winchester. 11 — No device.	Selects the device located at port 07CH (174Q), plugs P506 and P512.
3,2		00 — Soft-sectored 5.25-inch disk. 01 — H/Z-47 eight-inch floppy. 10 — Z-67 Winchester. 11 — No device	Selects the device located at port 078H (170Q), plugs P504 and P510, or P505 and P511.
4		0 — Primary boot from device at 07CH. 1 — Primary boot from device at 078H.	Determines whether the primary boot device is at port 07CH (174Q) or at 078H (170Q). The port not configured as primary becomes the secondary device.
5		0 — Initiate memory test on power up. 1 — Disable memory test on power up.	Disables/enables memory diagnostic on power up.
6		0 — Set console baud rate at 9600 (normal). 1 — Sets console baud rate at 19,200 (not currently supported).	Sets console baud rate.
7		0 — Normal. 1 — Auto-boot on power up.	Sets auto-boot.