RECALIBRATION

You will need the following equipment to calibrate your Disk Controller Board:

- A Digital Volt Meter (DVM) with 3-1/2 digit readout.
- A calibrated oscilloscope with sweep speeds of 100 ns/cm and 200 ns/cm, and an operating scale of 5 V peak-to-peak.
- A Frequency Counter capable of measuring 2.00 MHz. (Optional, but preferred).
- HDOS with INIT or CP/M with FORMAT software.

If you cannot obtain the proper results in the following steps, refer to the "In Case of Difficulty" section of this manual and correct any difficulties before proceeding.

Refer to Pictorial 7 when you perform the "Recalibration."

VCO BIAS ADJUSTMENT

Warm up the computer for a minimum of 15 minutes with the lid closed.

Connect your DVM to test point 1 on the H-/Z-89-37 board; connect the negative lead to ground and the positive lead to test point 1. The reading should be 1.38 to 1.42 V (this is the VCO bias voltage). If you do not obtain the proper voltage, adjust control R10.

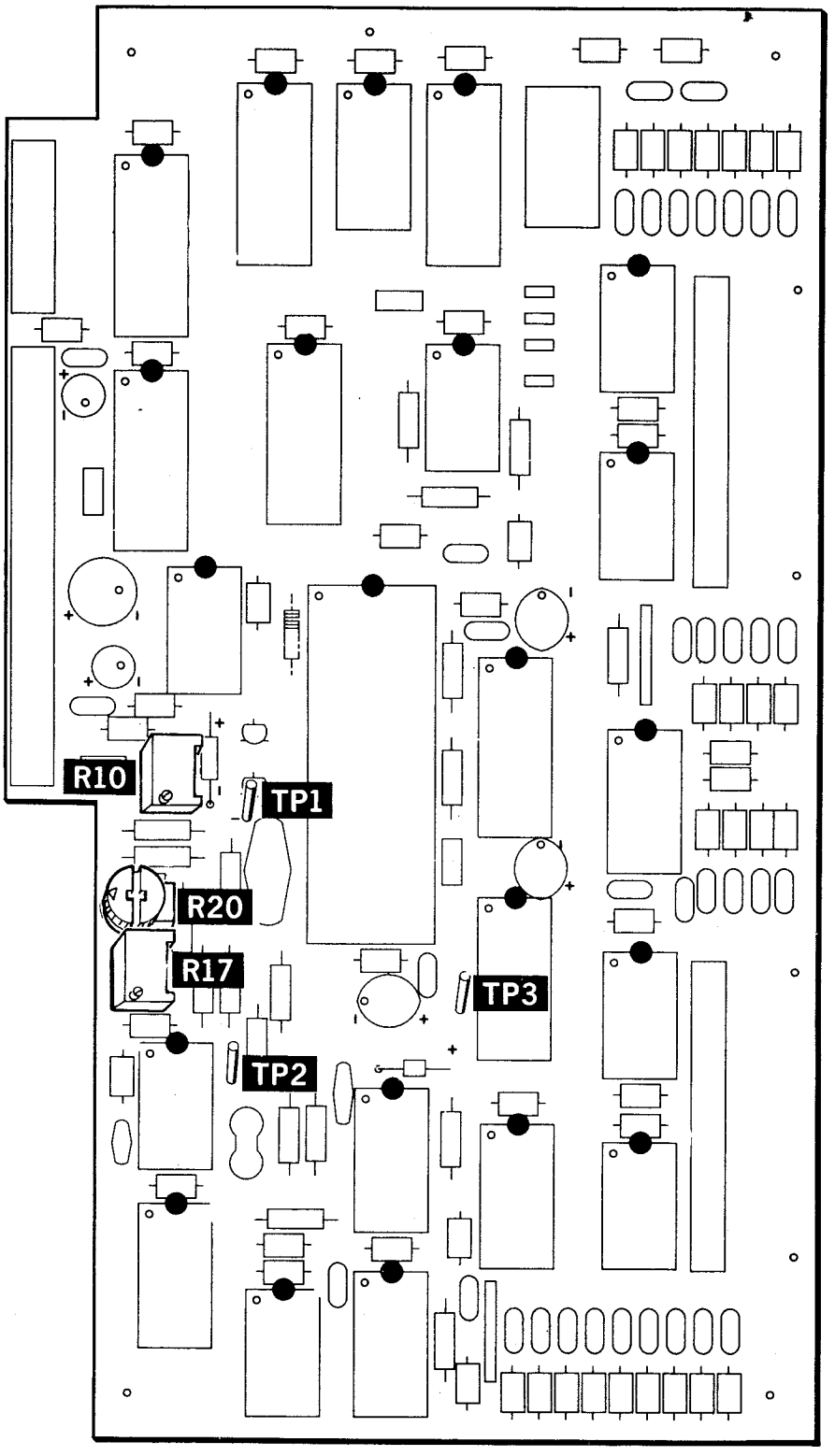
Disconnect the DVM.

VCO CENTER FREQUENCY ADJUSTMENT (WITH FREQUENCY COUNTER)

This is the preferred method of adjusting the VCO's center frequency.

Connect the frequency counter to test point 2 on the board. Set the counter to the 100 ms time base. The counter should read from 1975 to 2025 kHz. If it does not, adjust control R17.

Disconnect the counter.

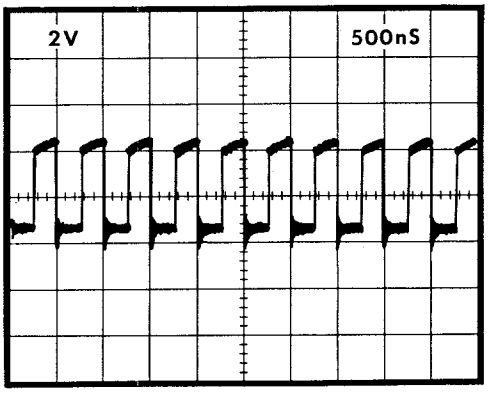


PICTORIAL 7

VCO CENTER FREQUENCY ADJUSTMENT (WITH OSCILLOSCOPE)

Connect the oscilloscope's input lead to test point 2.

Set the oscilloscope's sweep to 500 ns/cm. The period of the square wave displayed on the screen should be 493 to 506 ns. If it is not, adjust R17. See Pictorial 8.



PICTORIAL 8

Disconnect the oscilloscope.

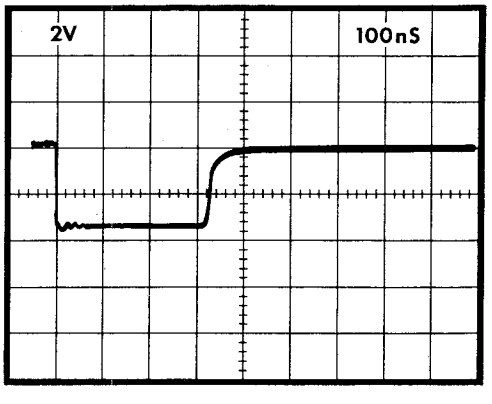
PRECOMPOSITION ADJUSTMENT

Connect the oscilloscope to test point 3.

Set the oscilloscope's sweep to 100 ns/cm.

Using your system's software (INIT in HDOS and FORMAT in CPM), write on the disk in double-density mode. The period of the pulse displayed on the screen should be 275 to 325 ns. If it is not, adjust control R20. See Pictorial 9.

NOTE:
MAY USE CPM FORMAT
FOR THIS TEST IN
D.S.D.D. MODE



PICTORIAL 9

Disconnect the oscilloscope.

This completes the calibration of your disk controller board.

CIRCUIT DESCRIPTION

The block diagram shows how the different parts of the disk controller board relate to each other (Illustration Booklet, Page 4).

The board's function is to translate the instructions of the processor to the disk drives. Assume that the processor wants to write on disk drive number one. First, the processor sends the proper enabling and control signals over the control lines. These signals are made compatible with the 1797 disk controller (U12) by the control decoder and inverter. The controller then blocks all interrupts to the processor (except its own) by sending a "block interrupts" signal to the interrupt control ICs. This prevents another peripheral from interfering with the transfer of data between the processor and the disk drive. The controller also signals the buffer direction control IC (U78) to allow input from the processor to pass through the data buffer to the controller.

The interface control latch then starts the disk drive motors by translating the drive control signals from the processor. The data from the processor is now sent through the data bus, the 1797, the support logic and disk interface logic, and to drive number one over the disk serial data line (the support logic and disk interface logic help the 1797 disk controller communicate with the drive electronics). The support logic consists of ICs U8B, U13, U14A, and U15. The interface logic consists of U19, U20, U21, and U22. These are all explained below.

The read process is similar to the write process. First, the processor sends the proper enabling and control signals over the control lines, just as before (of course this time the signals enable the disk controller board to read instead of write). The signals are made compatible with the 1797 disk controller IC by the control decoder and inverter. The controller again blocks all interrupts to the processor (except its own) by sending a "block interrupts" signal to the interrupt control ICs, preventing another peripheral from interfering with the transfer of data. The controller also signals the buffer direction control IC to allow output (to the processor) to pass through the data buffer from the controller. The interface control latch then starts the disk drive motors by translating the drive control signals from the processor. The data from the disk is now sent over the drive serial line, through the disk interface logic, the support logic and the 1797 disk controller, and to the processor via the data buffer and data bus.

The phase lock loop (PLL), which is part of the support logic, and the variable control oscillator (VCO) together track the frequency of data read from the disk. This tracking generates a read clock (RCLK) signal that tells the disk controller how fast to read the data. (The frequency of the incoming read data changes due to variations in the rotating speed of the disk and the position of the data on the disk.)

CONTROL LINES (P2)

Please refer to the schematic diagram while you read this description.

All of the disk control lines from the processor are input to U6 via plug P2, except for the processor system clock line, which is input to U5A via pin 13 of P2.

The control lines consist of address lines A0, A1, and A2, read line RD, write line WR, I/O DISK, I/O FLPY, and the reset line RESET. (Address line A2 is inverted by U5B when J1A is jumpered. J1A is jumpered in the standard operating mode, as is J2A. Otherwise A2 goes directly to U6.) The address lines access the 1797 disk controller's (U12) registers. The read and write lines, low when active, tell the controller which way the data buffer direction control should be set and whether the read or write lines to the disk driver electronics should be used. The I/O DISK and I/O FLPY lines enable the controller board and tell the board which block of memory in the processor is used for disk I/O. The I/O DISK line is used in the standard mode. In this mode, the I/O memory block base address is 170 octal. I/O FLPY, when connected through jumper J2B, is used when the programmer wishes to designate another block of memory for disk I/O. The last control line, RESET, initializes the controller.

U1 DATA BUFFER AND U7B BUFFER DIRECTION CONTROL

The data buffer is a bidirectional, eight-bit buffer whose direction is controlled by U7B, the buffer direction control.

U2, U3, AND U4 INTERRUPT CONTROL

IC's U2 and U4 are taken from the processor CPU board. They are the processor's interrupt channels. They are relocated onto the disk controller board so that the disk controller can block all other interrupts to the processor except its own. U3 screens the interrupt signals to the processor under U11's direction. U3 turns the eight-bit interrupts to the processor into three-bit interrupt signals. The three-bit interrupt becomes part of an eight-bit data instruction via U2. U2 supplies five other hard wired bits.

For more information about U2 and U4, consult your processor's operation manual.

U5 OPEN COLLECTOR NAND GATES

There are four gates used on the IC, called A, B, C, and D. The gates invert the: processor system clock for use by the 1797, interrupts from the 1797 to the processor, and addressing information from the processor to all parts of the disk controller board.

U6 CONTROL DECODER AND INVERTER

U6 is a programmable logic array, designed to decode address and read and write conditions for the controller board. Using addresses A0, A1, and A2 it determines whether the board is being addressed, which register is being addressed, and whether the signal is a read enable or write enable signal.

The internal logic of U6, and most other ICs on the board, are shown in the "Semiconductor Identification Chart" (Page 61). All inputs and outputs of the IC are marked on the chart as they are on the schematic.

U7A ADDRESS CONTROL LATCH

The address control latch helps call up the registers in the 1797 — either the track and sector registers or the C/S and data registers, depending on how data bit 0 is set on the interface control latch.

U8A RESET PULSE LATCH

The reset pulse from the processor does not meet the minimum reset pulse requirements of the 1797. To correct this, U8A lengthens the reset pulse to an interval sufficient to meet the 1797's specifications. U8A also supplies the reset signal to U16, part of the phase lock loop circuitry. U16 then resets the precompensation clock generator, U18.

U8B HEAD LOAD DELAY

U8B is a monostable multivibrator that delays the controller's response to commands. This allows the drive head to settle after it is selected.

U9 and U10 DISK CONTROLLER CLOCK

U9 is a clock oscillator that runs at 16 MHz. The output of U9 is fed to U10. U10 divides U9's output by 16, producing a 1 MHz clock signal with a 50% duty cycle.

U11 INTERFACE CONTROL LATCH

The U11 is an octal type-D latch. It latches the high speed processor signals for the 1797 disk controller (U12) and interface control latch (U11). Some commands, such as MOTOR, go directly from the U11 to the disk drive interface ICs, U19, U20, and U21, rather than through the 1797.

U12 1797-02 DISK CONTROLLER

The internal logic of the 1797 is discussed in Appendix A. Refer to the appendix for information about the 1797's operation.

U13 INPUT SIGNAL MULTIPLEXER

This IC multiplexes the control and data signals from the two disk interfaces into the disk controller board. The multiplexer switches between the two interface line groups, depending on which drive is selected and on which of jumpers J4, J5, J6, or J7 is set. The multiplexer isolates the two drive interfaces to prevent their interfering with each other.

U14 RAW READ LATCH

U14 lengthens the raw read pulse from the disk drive electronics to a size readable by the 1797 (U12).

U15 DRIVE BUFFER

U15 buffers the control and data signals to the two drive interfaces.

U16, U17, U18, Q1 and Q2 PHASE LOCK LOOP TRACKING AND PRECOMPENSATION

U16 supplies U17 with either a pull-up (PU) or pull-down (PD) signal. This signal is then filtered by C29 and R13 and then called FC — frequency control. Voltage control oscillator U17 changes its frequency, higher with a PU signal and lower with a PD signal. The change in frequency produces a corresponding change in rotational speed of the disk.

Variable resistor R10 biases the PU and PD output at 1.4 volts (this means that PU/PD are 1.4 volts when the Phase Lock is inactive). This allows the phase lock to more quickly lock on to the data being read. Variable resistor R17 adjusts the VCO's center frequency to 2 MHz.

The VCO's output is divided down by U16. This signal then becomes the read clock (RCLK) signals, which is used by the 1797 to separate disk data and disk clock signals.

The U16 also strobes the early and late signals for data precompensation. These internally latched signals determine which phase of a four-phase clock generator, U18, will be used for the precompensation process. All phases are identical in pulse width (+ or− 50 nsec). The phase delay time is set by R20.

Precompensation, used for 80-track double-density disk write operations, places data properly on the disk so that it can be read back with minimum error. (Error may be introduced by the shifting of old data as new data is written — as data is written, data adjacent to the new data is shifted over because of the nature of the magnetic medium of the disk.)

U18, precompensation clock generator, provides the clock signals needed for precompensation of write signals.

U19, U20, U21, AND U22 DISK DRIVE INTERFACE

The disk drive interface ICs buffer all signals to and from the disk drive electronics by means of open collector drivers.

U23 VOLTAGE REGULATOR

U23 supplies +5 V regulated to U17, isolating the U17 from the Z-89 +5 V power supply.

REPLACEMENT PARTS LIST

CIRCUIT Comp. No.	HE Part No.	DESCRIPTION
RESISTORS		
R1	6-102-12	1000 Ω, 1/4-watt
R2	6-103-12	10 kΩ, 1/4-watt
R3	6-103-12	10 kΩ, 1/4-watt
R4	6-102-12	1000 Ω, 1/4-watt
R5	6-102-12	1000 Ω, 1/4-watt
R6	6-104-12	100 kΩ, 1/4-watt
R7	6-103-12	10 kΩ, 1/4-watt
R8	6-102-12	1000 Ω, 1/4-watt
R9	6-103-12	10 kΩ, 1/4-watt
R10	10-1180	100 kΩ control
R11	6-473-12	47 kΩ, 1/4-watt
R12	6-473-12	47 kΩ, 1/4-watt
R13	6-680-12	68 Ω, 1/4-watt
R14	Not Used	
R15	Not Used	
R16	6-1002-12	10 kΩ, 1/4-watt
R17	10-1154	10 kΩ, 1/2-watt control
R18	6-1002-12	10 kΩ, 1/4-watt
R19	6-222-12	2200 Ω, 1/4-watt
R20	10-1138	10 kΩ, 3/4-watt control
R21	6-124-12	120 kΩ, 1/4-watt
R22	6-332-12	3300 Ω, 1/4-watt
RP1	9-120	150 Ω (5) resistor pack
RP2	9-120	150 Ω (5) resistor pack
CONNECTORS — CABLES		
P1	432-1074	10-pin connector
P2	432-1076	25-pin connector
P3	432-1053	34-pin connector
P4	432-1053	34-pin connector
	100-1817	20-pin plug w/jumper
	134-1158	16-conductor cable w/connectors
	134-1074	Short floppy cable
	134-1163	Long floppy cable

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION

CAPACITORS

C1-C16	21-769	.01 μF ceramic
C17	25-911	22 μF electrolytic
C18	21-769	.01 μF ceramic
C19	25-911	22 μF electrolytic
C20	21-769	.01 μF ceramic
C21	21-141	.0033 μF ceramic
C22	21-769	.01 μF ceramic
C23	21-769	.01 μF ceramic
C24	21-769	.01 μF ceramic
C25	21-769	.01 μF ceramic
C26	21-769	.01 μF ceramic
C27	20-188	30 pF mica
C28	21-769	.01 μF ceramic
C29	27-217	.68 μF Mylar*
C30	21-192	.1 μF ceramic
C31	25-195	2.2 μF tantalum
C32	21-744	82 pF ceramic
C33	21-192	.1 μF ceramic
C34	21-769	.01 μF ceramic
C35	25-197	1 μF tantalum
C36-C63	21-773	470 pF ceramic
C64	25-883	47 μF electrolytic
C65-C66	25-841	4.7 μF tantalum
C67	21-769	.01 μF ceramic
C68	25-841	4.7 μF tantalum
C69	21-769	.01 μF ceramic

INDUCTORS

L1-L8	235-229	35 μH, RF Choke
L9		Not Used
L10-L37	235-230	7 μH, Ferrite Core

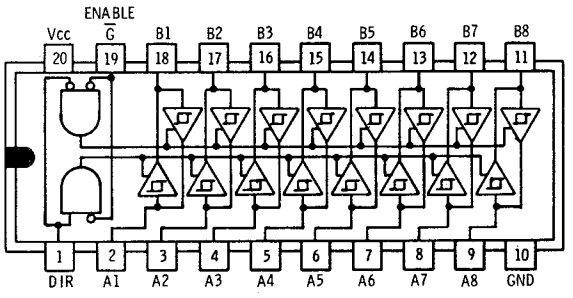
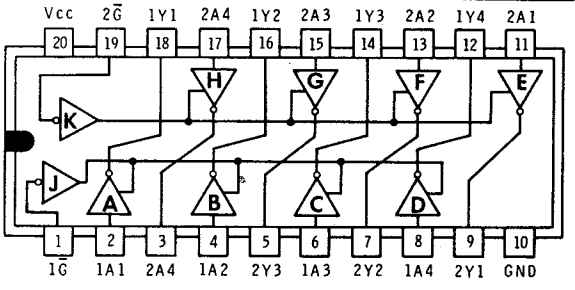
INTEGRATED CIRCUITS

See the "Semiconductor Identification Charts."

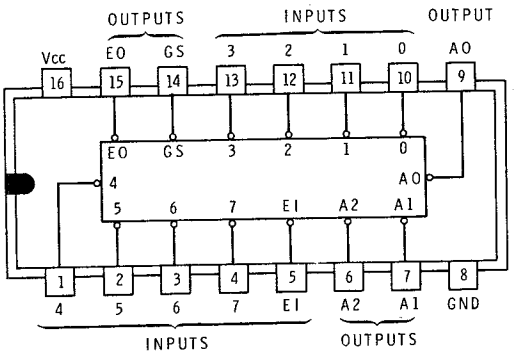
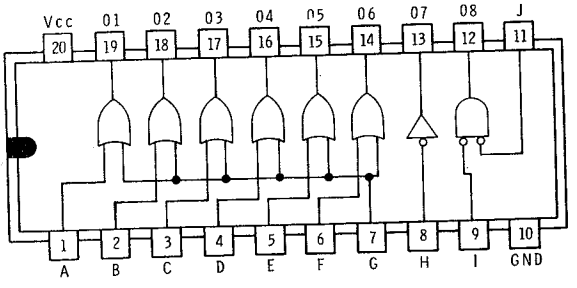
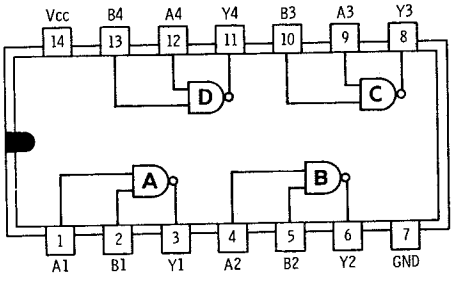
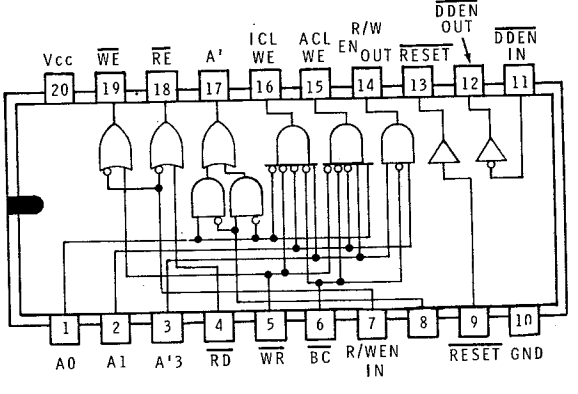
*DuPont Registered Trademark.

SEMICONDUCTOR IDENTIFICATION CHART

INTEGRATED CIRCUITS

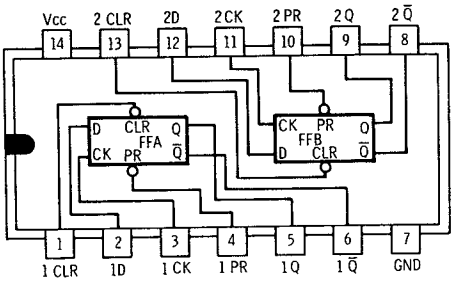
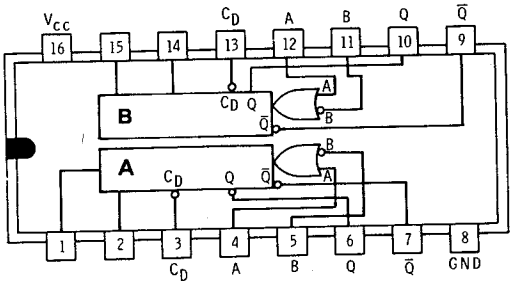
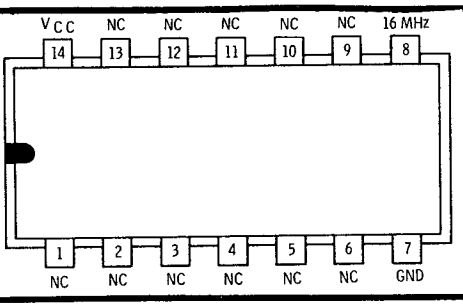
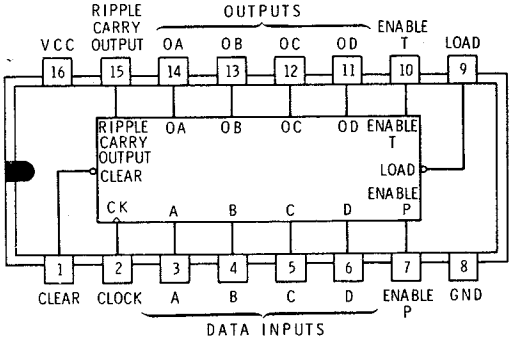
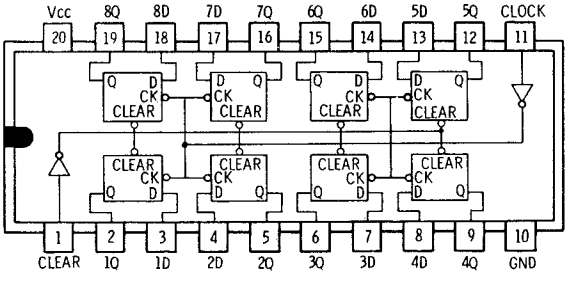
COMPONENT NUMBER	HE PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
U1	443-885	74LS245	
U2	443-754	74LS240	

Integrated Circuits (Cont'd.)

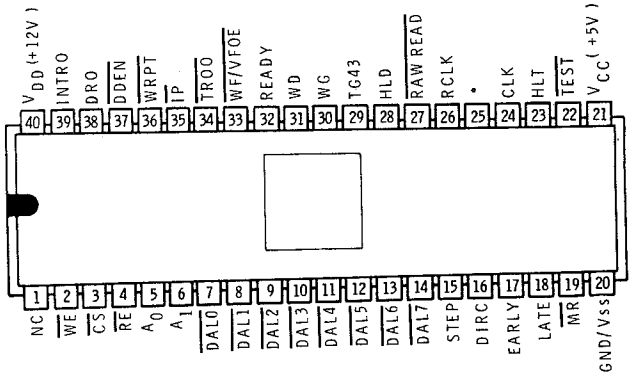
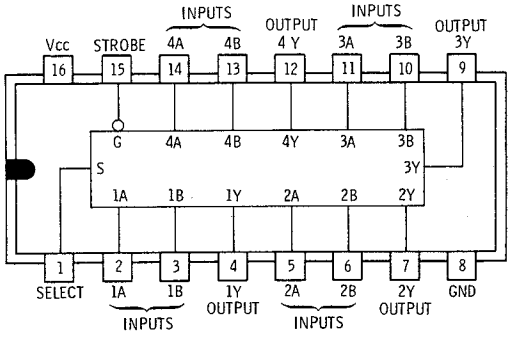
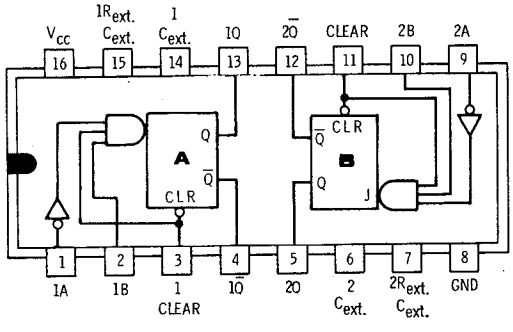
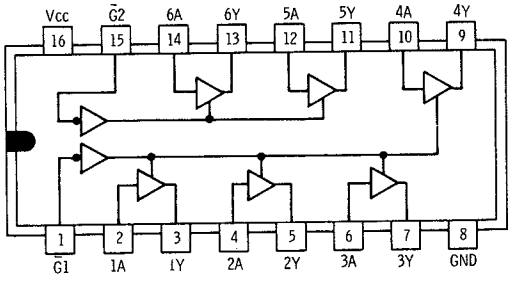
COMPONENT NUMBER	HE PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
U3	443-912	74LS148	
U4	444-82	*	
U5	443-745	74LS03P	
U6	444-81	*	

*Only available from Heath Co.

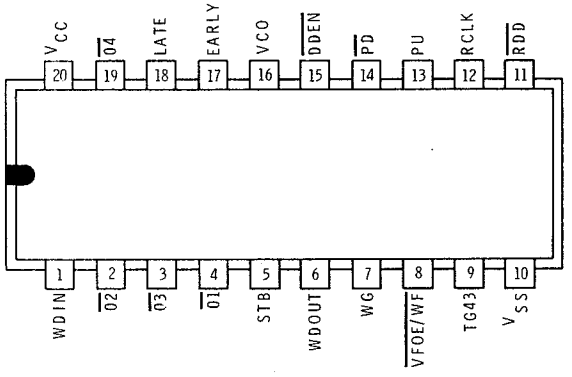
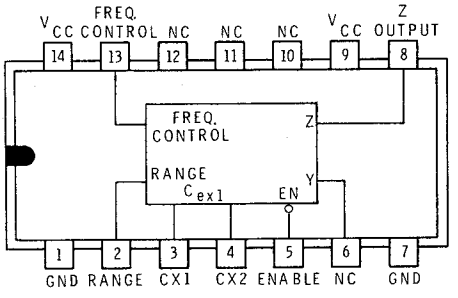
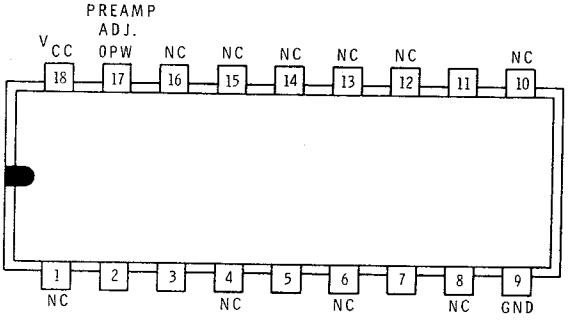
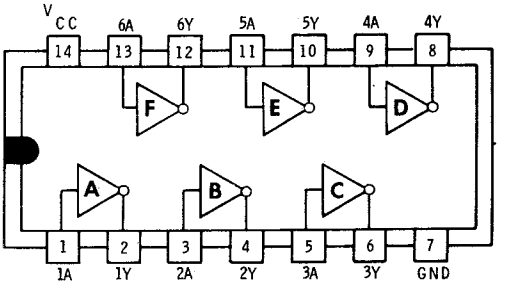
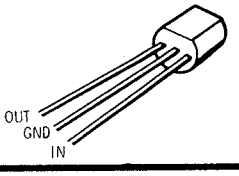
Integrated Circuits (Cont'd.)

COMPONENT NUMBER	HE PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
U7	443-730	74LS74	
U8	443-727	96L02	
U9	150-107	LOCO II 16 MHz Osc.	
U10	443-757	74LS161	
U11	443-805	74LS273	

Integrated Circuits (Cont'd.)

COMPONENT NUMBER	HE PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
U12	443-997	WD1797-02	
U13	443-799	74LS157	
U14	443-90	74123N	
U15	443-857	74LS367	

Integrated Circuits (Cont'd.)

COMPONENT NUMBER	HE PART NUMBER	MAY BE REPLACED WITH	IDENTIFICATION
U16	443-998	WD1691	
U17	443-999	74LS624	
U18	443-1000	WD2143-03	
U19, U20, U21, U22	443-73	7416N	
U23	442-627	78L05	

Appendix A

FD179X DATA INFORMATION

The following pages are reprinted with the permission of Western Digital Corporation.

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

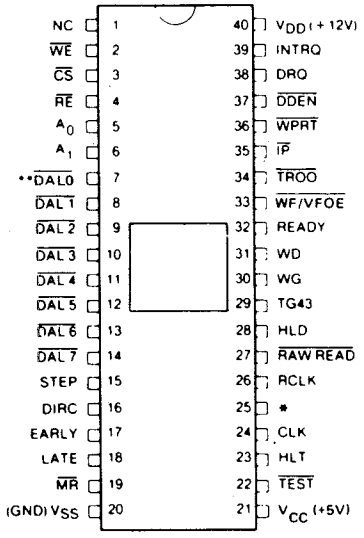
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  IBM 3740 Single Density (FM)
  IBM System 34 Double Density (MFM)
- READ MODE
  Single/Multiple Sector Read with Automatic Search or Entire Track Read
  Selectable 128 Byte or Variable length Sector
- WRITE MODE
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  Selectable Track to Track Stepping Time
  Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

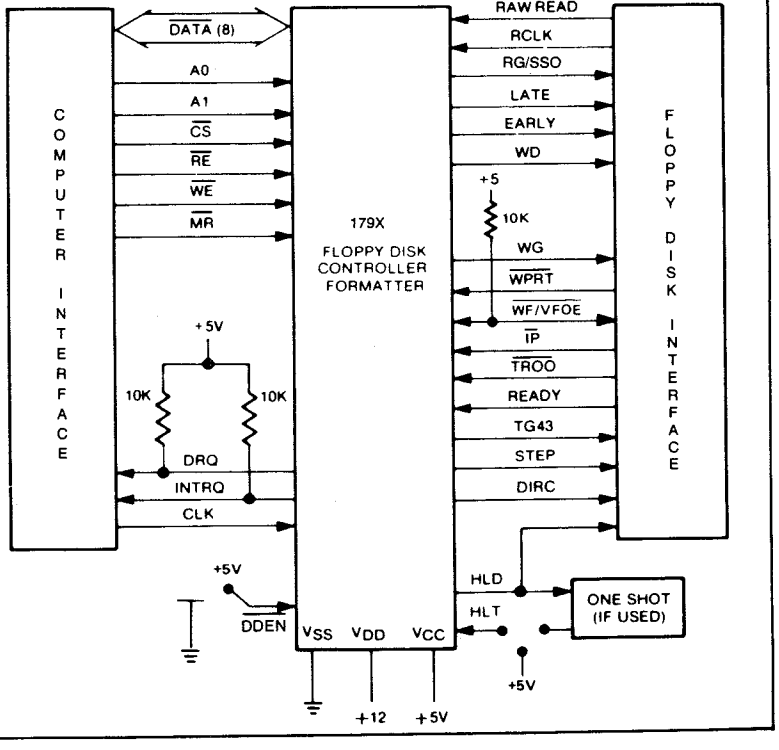
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control:
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

A1	A0	$\overline{\text{RE}}$	$\overline{\text{WE}}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / VFO ENABLE	$\overline{\text{WF}}$/$\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

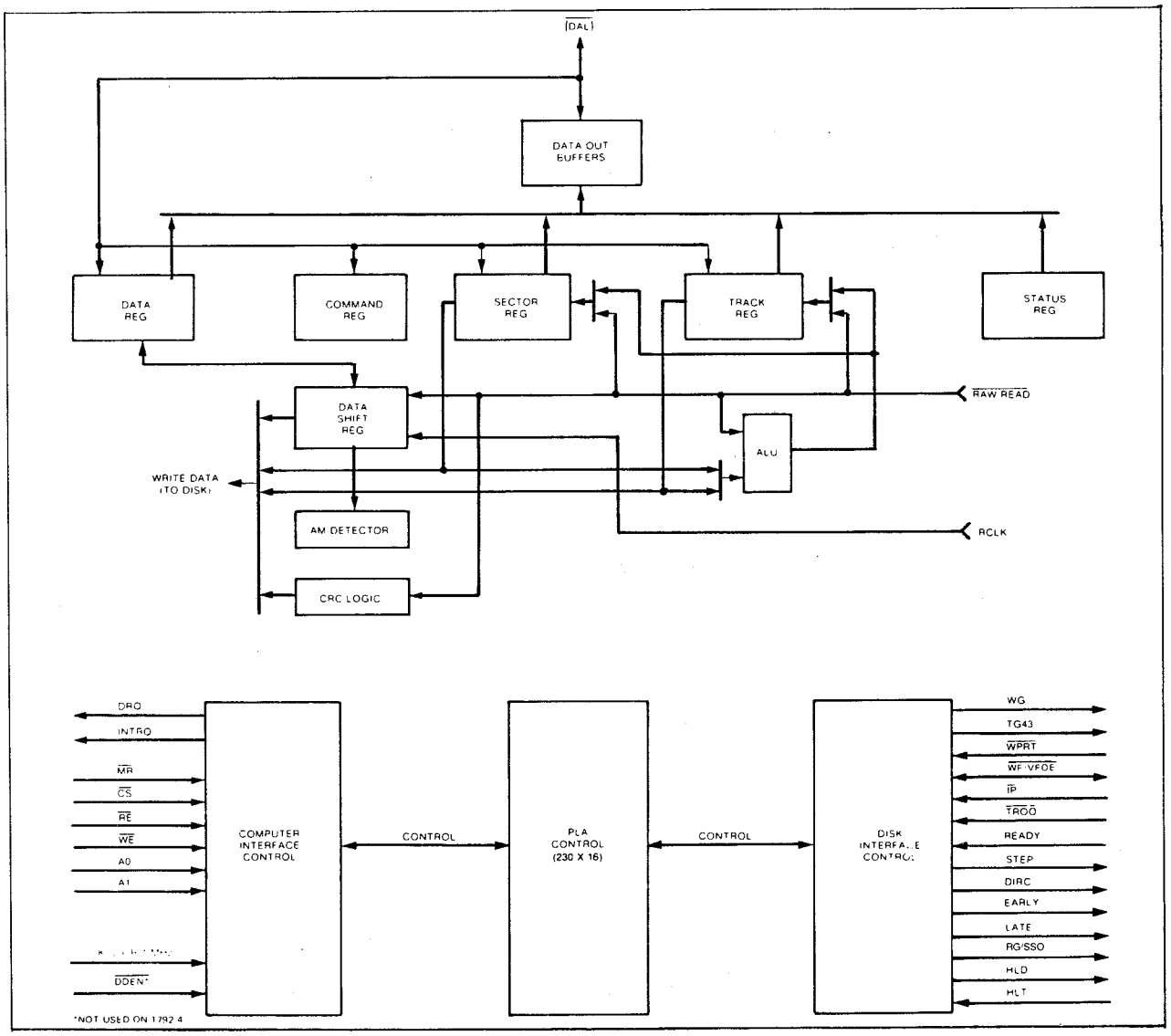
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

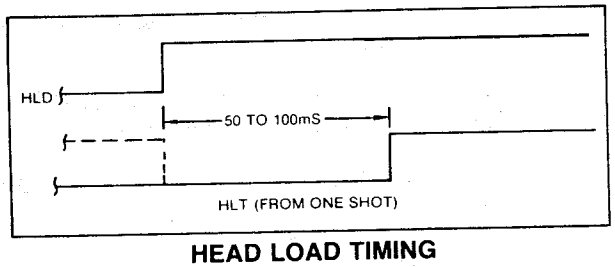
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{RAW}$ $\overline{READ}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 250 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0
S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare
C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0
S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
I_3 -I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

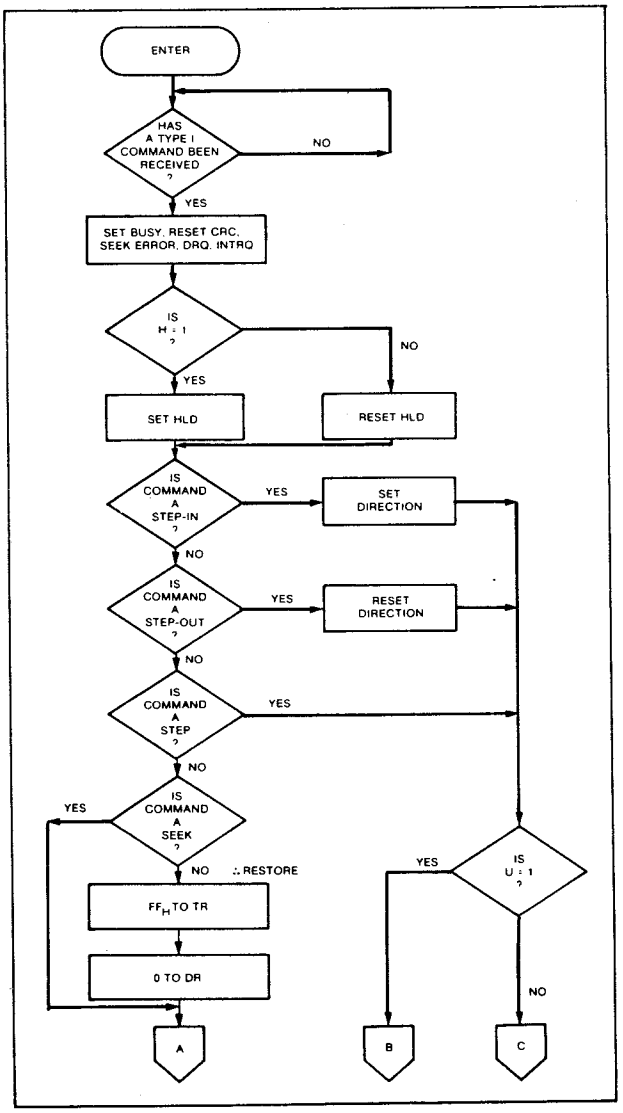
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

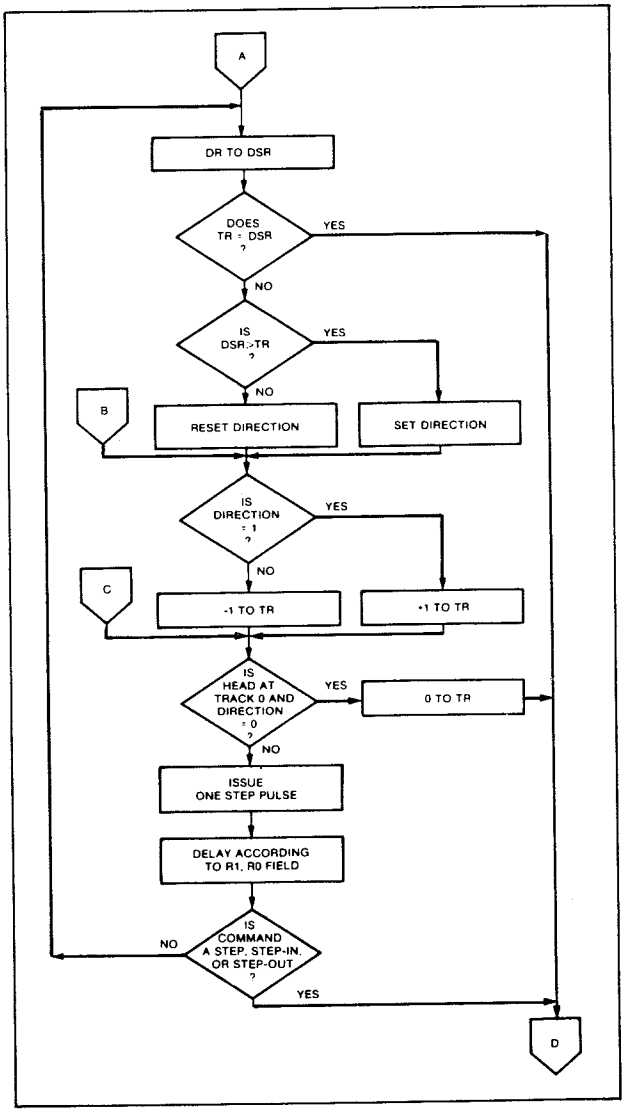
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



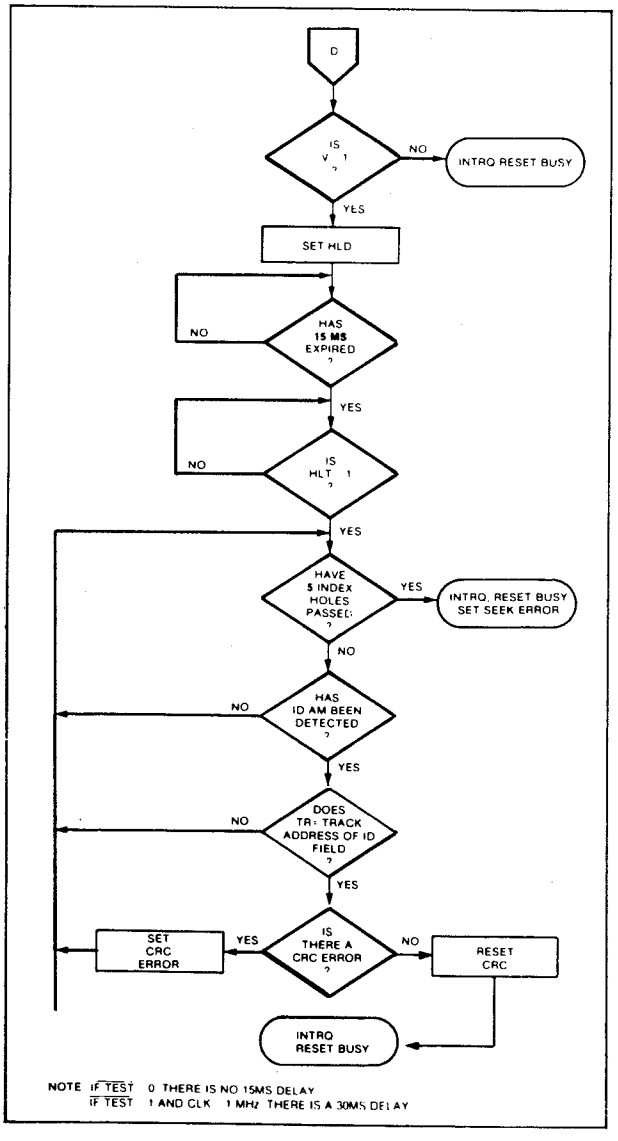
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TROO}$) input is sampled. If $\overline{TROO}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TROO}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TROO}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TROO}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

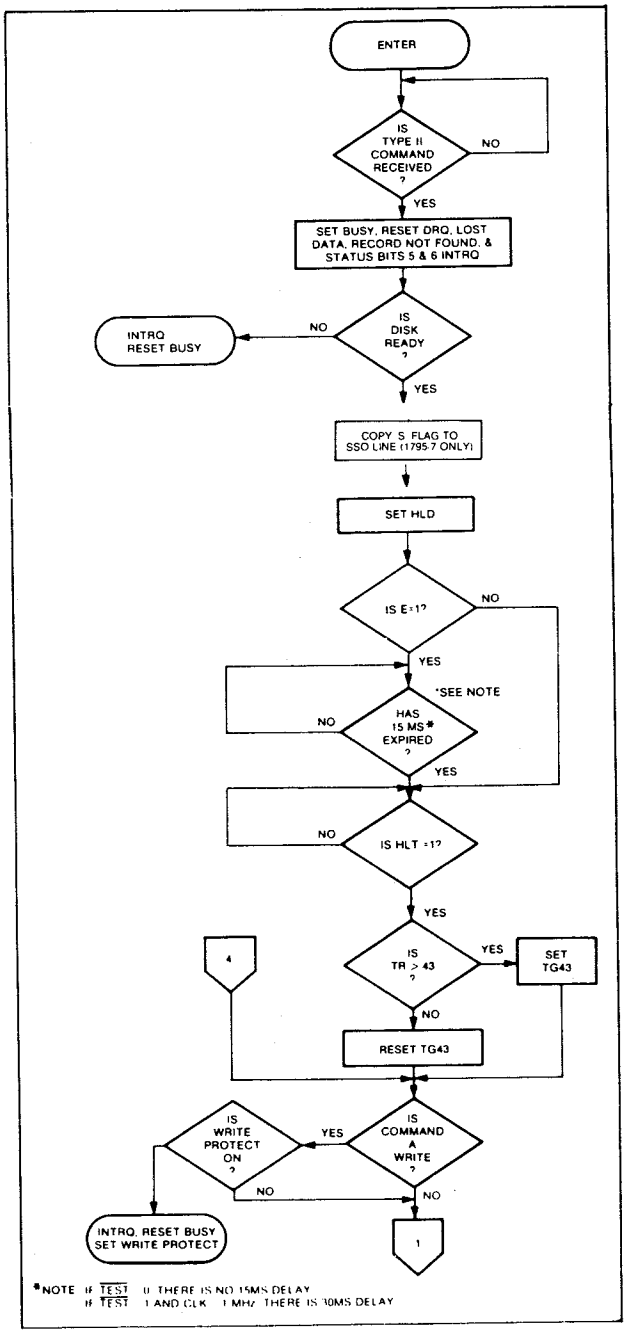
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

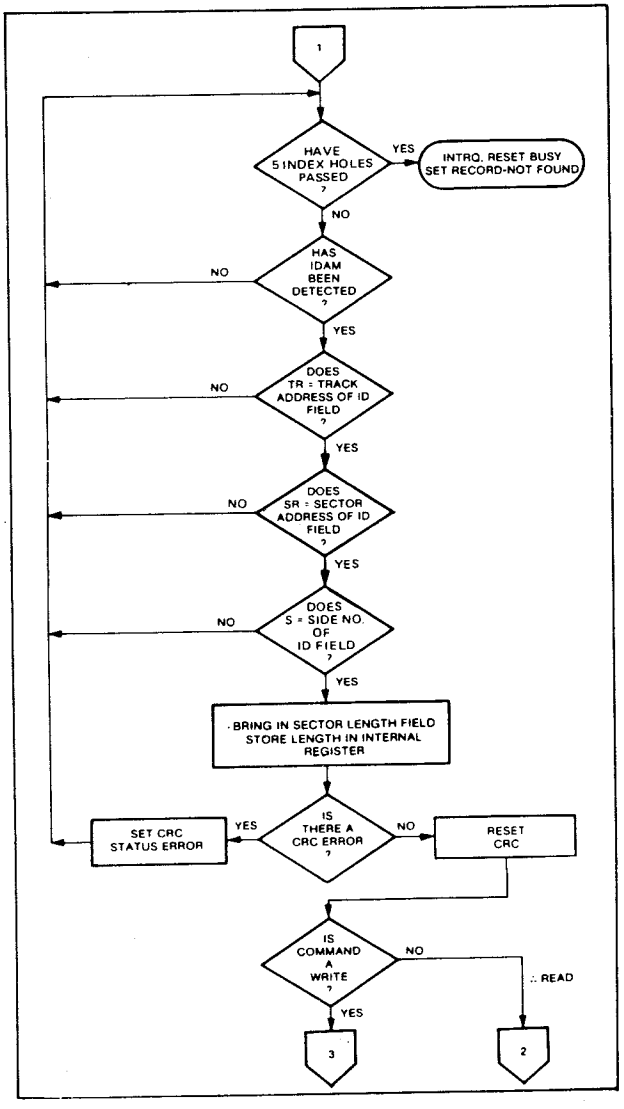
countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

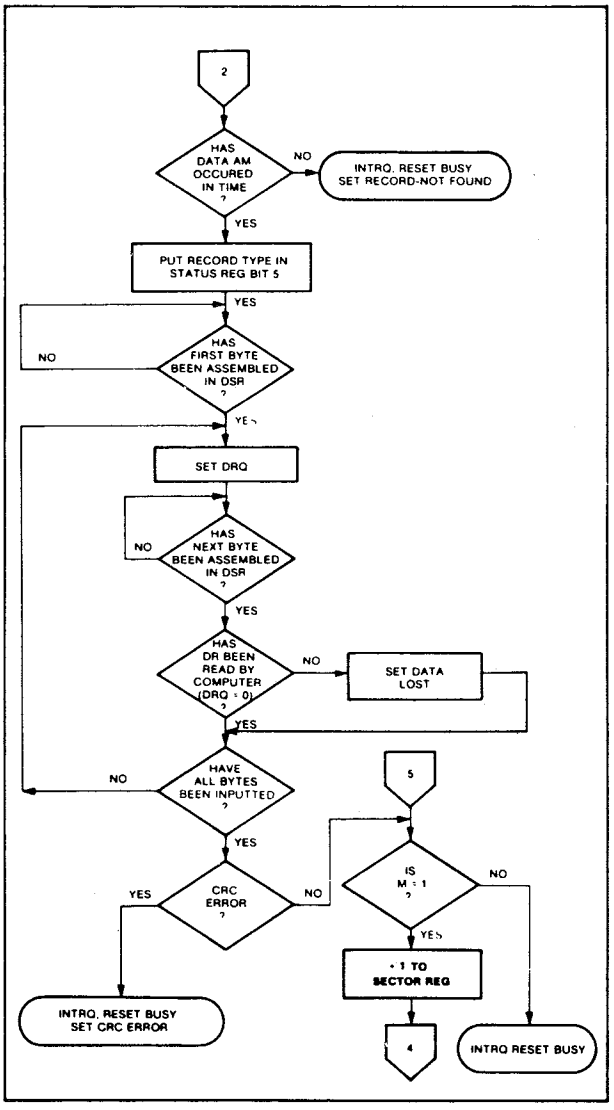
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

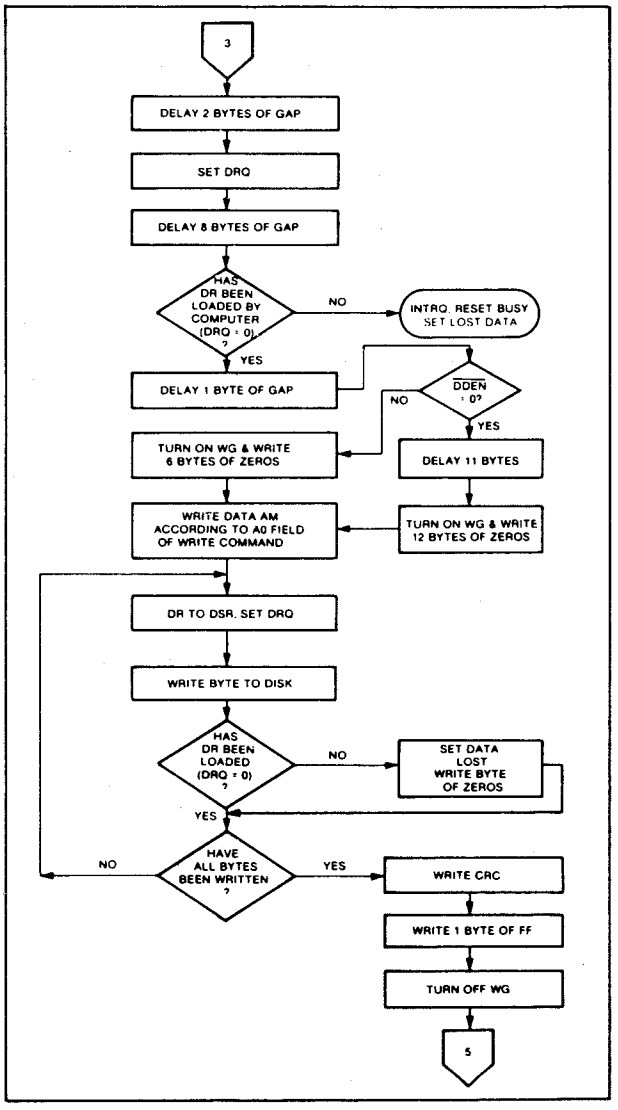
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

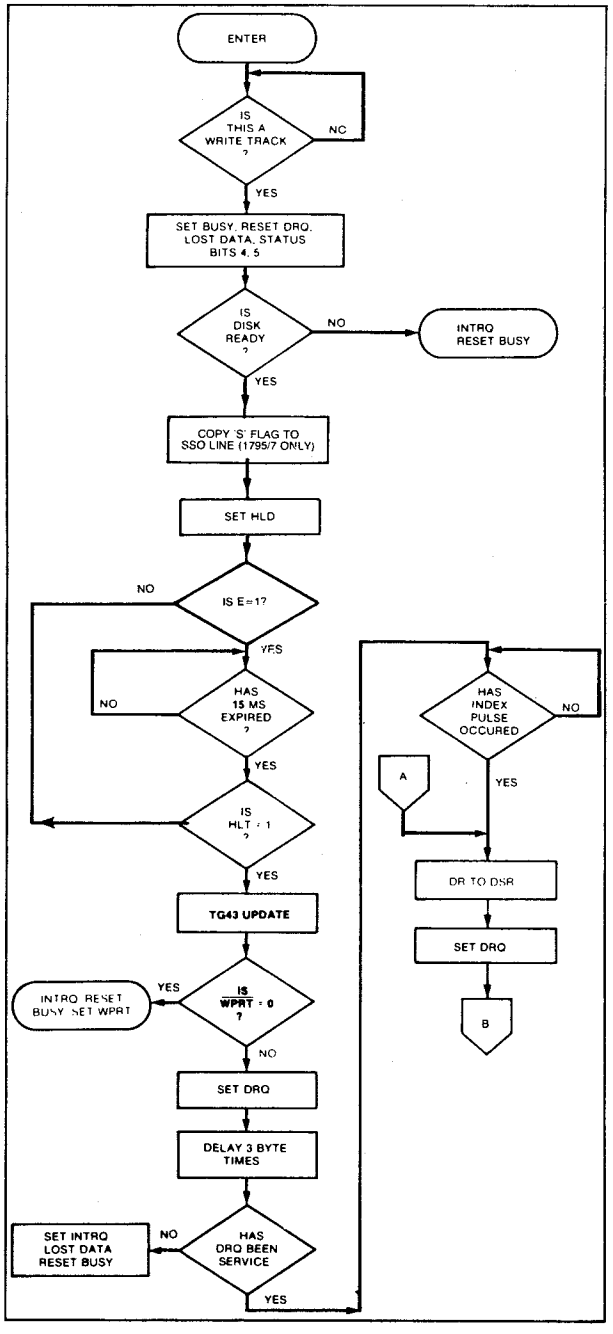
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

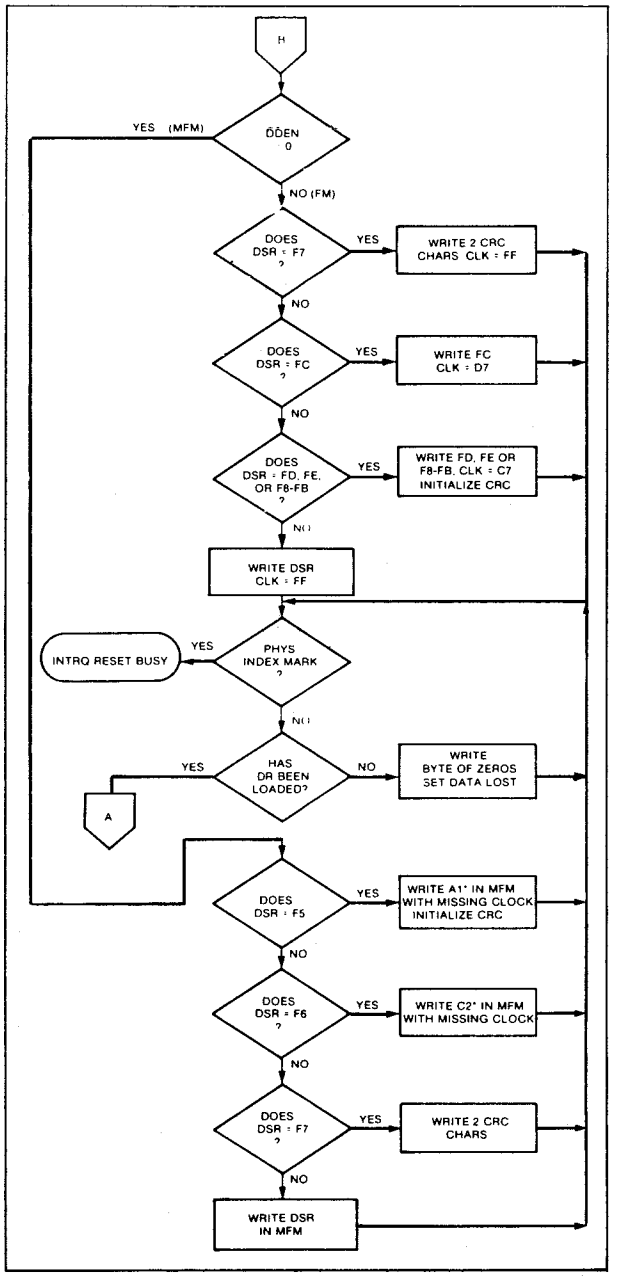
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND WRITE TRACK



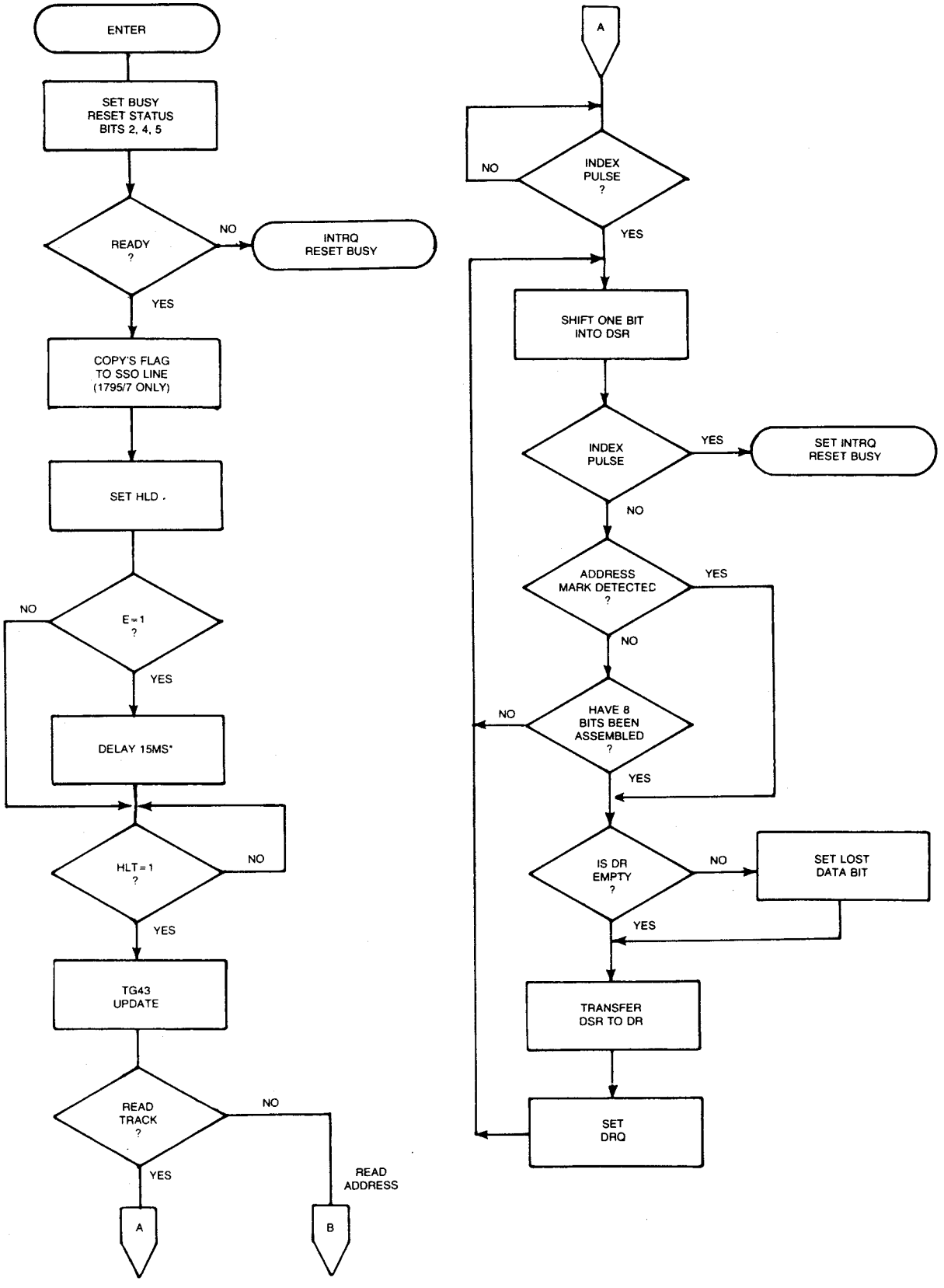
TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4



*If TEST = ϕ NO DELAY

If TEST = 1 and CLK = 1 MHZ, 30 MS DELAY

TYPE III COMMAND

Read Track/Address