



MONITOR MTR-90

595-2696-02

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INTRODUCTION

This Manual describes the functions and operation of the Z-89/90 Monitor Program, MTR-90, which is contained in a read-only memory (ROM) on the Z-89/90 CPU board. Some of the major features of MTR-90 include:

- Disk system bootstrap routines.

- Memory contents display and alteration.

- Program execution control.

- Variable radix settings for display addresses and conversion.

- Input/output to specified ports.

- Memory diagnostic routine.

In addition, by means of a flag byte maintained in read/write memory, MTR-90 can be instructed to bypass some or all of its normal functions. In this manner, a sophisticated user can augment or replace these functions.

THEORY OF OPERATION

This section supplements information in the "Operations" and "Circuit Description" sections of your Z-89/Z-90 Operations Manual. In order to use all of the features of MTR-90, it is necessary to understand the 8080 and Z-80 opcodes and the circuitry of your Z-89/90. This section details the operation of MTR-90. For a listing of the MTR-90 program, see Appendix A.

Power Up and Reset

MTR-90 initializes the Z-89/90 whenever you apply power to or reset the computer. To power up, use the switch on the right rear of the Z-89/90. To reset, simultaneously press the RESET key and the right-hand shift key on the keyboard. When reset, MTR-90 sounds the electronic "bell" and displays the "H:" prompt on the terminal screen.

During the initialization procedure, MTR-90 determines the high limit of continuous RAM. Once MTR-90 has established this high memory limit, the Z-80 stack pointer is set to the value of the upper memory limit. Then MTR-90 enters a loop and awaits a command.

General Operations

When you power up or reset your Z-89/90, MTR-90 responds by clearing the screen and displaying "H:". This "H:" prompt informs you that MTR-90 is ready to respond to commands. When you enter a character, MTR-90 will either accept it, completing a command word, or beep, which signifies an invalid command word or an inability to boot.

The DELETE key kills a partially entered line and causes MTR-90 to return the "H:" prompt. This is useful for correcting typing errors.

Clock Interrupts

The clock interrupt is a crucial element in the operation of the Z-89/90. It is a level one interrupt, and is generated on the Z-89/90 CPU board every two milliseconds. MTR-90 maintains a tick counter called "TICCNT", which counts one tick every 2 milliseconds. Refer to the listing in Appendix A for the location of TICCNT.

Note that MTR-90 uses interrupts, so you should not disable interrupts using the DI instruction for other than very short periods of time. MTR-90 also requires a stack pointer at the top of memory with at least 80 bytes of stack area.

NOTE: In this manual, the symbol Δ means press the space bar and \oplus means press the RETURN key.

MTR-90 COMMANDS

The following section summarizes valid commands to MTR-90. Each command is listed in alphabetical order along with a brief explanation and examples. You need only enter the first letter of these commands — MTR-90 will respond with what is enclosed in parentheses. In most cases, you will need to press RETURN before MTR-90 will respond. Where a command requires numeric input, we have used the hexadecimal, octal, and split octal number bases.

B(oot)


Typing B(oot) and pressing RETURN initiates boot from drive 0 of the disk drives which have been configured for primary boot using SW501 switch 4 (see Appendix D). This command may optionally be followed by a unit number which specifies a drive other than drive zero. The unit number may be optionally followed by a command string which begins with a colon. The command string is currently used only by those Heath/Zenith operating systems which support the H/Z-67 Winchester disk subsystem. For more detailed information about how MTR-90 accomplishes bootstrap, see Appendix A.

If the boot fails, the computer will display a question mark, beep, and display the H: again. The possible causes for a boot failure include:


1. The boot device is not activated within 15 seconds.
2. The DELETE key is pressed during boot.
3. Switch SW501 is not set properly.
4. A disk error occurs.

The DELETE Key cancels the B(oot) command and repeats the H: prompt, unless boot has already begun, in which case the system displays the message “?Boot Error”.


EXAMPLE 1: Boot from unit zero of the primary boot drives.

H: B(oot) 

EXAMPLE 2: Boot from unit 2 of the primary boot drives.

H: B(oot)2 

EXAMPLE 3: Boot from primary boot Z-67 unit 2, passing the command line "HDOS;1" to the secondary Z-67 boot routine.

H: B(oot)2:HDOS;1 

B(oot) S(D)


The B(oot) S(D) command initiates boot from unit zero of the drives which have been configured using SW501 switch 4 as secondary boot drives (see Appendix D). This command may optionally be followed by a unit number which specifies a drive other than drive zero. The unit number may be optionally followed by a command string which begins with a colon. The command string is currently used only by those Heath/Zenith operating systems which support the H/Z-67 Winchester disk subsystem.

If the boot fails, the computer will display a question mark, beep, and display the H: again. The possible causes for a boot failure are:


1. The boot device is not activated within 15 seconds.
2. The DELETE key is pressed during boot.
3. Switch SW501 is not set properly.
4. A disk error occurs.

The DELETE key cancels the B(oot) S(D) command and repeats the H: prompt, unless boot has already begun, in which case the system prints the message "?Boot Error".

EXAMPLE 1: Boot from secondary boot drives, unit zero.

H: B(oot) S(D) 

EXAMPLE 2: Boot from unit 2 of the secondary boot drives.

H: B(oot) S(D)2 

EXAMPLE 3: Boot from secondary boot Z-67 unit 2, passing the command line "HDOS;1" to the Z-67 boot routine.

```
H: B(oot) S(D)2:HDOS;1 Ⓢ
```

C(onvert)

The C(onvert) command converts a sixteen-bit number specified in the opposite radix to the current radix. To set the current radix, see the **R(adix)** command on Page 9.

EXAMPLE: Convert FFFF hex to split octal, where octal is the current radix.

```
H: (C(onvert)FFFF Ⓢ
377377
H:
```

G(o)

The G(o) command initiates a user program, beginning at the address specified in the current radix as an argument to the G(o) command. If no argument is supplied with the G(o) command, then execution begins at the address contained in the program counter.

EXAMPLE: Go to address 40200 octal.

```
H: G(o)40200 Ⓢ
```

I(n)

I(n) inputs a number from the port specified as an argument to the I(n) command. The port number must be specified in the current radix.

EXAMPLE: Input data from port 177 octal, where octal is the current radix.

```
H: I(n)177 Ⓢ
370
H:
```

O(ut)

The O(ut) command outputs the specified data to the specified port. The first number is the port, and the second the data. Both values should be expressed in the current radix, and should be separated by a comma.

EXAMPLE: Send FF out port A7, where hex is the current radix.

```
H: O(ut)A7,FF  Ⓢ
```

P(rogram Counter)

The P(rogram Counter) command sets the current address in the program counter. This command is used to specify the object of the G(o) command. The address specified should be expressed in the current radix.

Simply typing P and RETURN causes the system to display the current contents of the program counter and then to await a new value. Typing P followed by a value sets the PC to that value. Typing P and RETURN, then pressing RETURN again without entering a value terminates the command and does not alter the PC.

EXAMPLE 1: Set the program counter to 100 hex, where the current radix is hexadecimal.

```
H: P(rogram Counter) 100  Ⓢ
H:
```

EXAMPLE 2: Display the contents of the program counter without altering its contents.

```
H: P(rogram Counter)  Ⓢ
FFFF  Ⓢ
H:
```

EXAMPLE 3: Set the program counter to 40100 octal after examining the current value, where the current radix is octal.

```
H: P(rogram Counter)  Ⓢ
377377 40100
H:
```

Note that the operator entered the 40100 in this example.

R(adix)

The R(adix) command sets the current working radix for all other commands.

Valid arguments to radix are O(ctal) and H(exadecimal). The default current radix on power up is octal. Typing R and RETURN with no argument displays the current radix.

EXAMPLE: Set the current radix to hexadecimal and then check it.

```
H: R(adix) H(exadecimal)
H: R(adix)      CR
Hexadecimal
H:
```

S(ubstitute)

The substitute command can be used to examine or alter the contents of a memory location. The argument to S(ubstitute) is the first address to be examined (and optionally changed). When the starting address has been entered and terminated by pressing RETURN, the system displays address/value pairs. To replace the old value with a new one, type a new value, then a space. To proceed to the next memory location, type a space without entering anything else. To examine a previously displayed memory location, type a hyphen. To terminate, press RETURN.

EXAMPLE: Modify address 40100 octal, where octal is the current radix, then check the memory location.

```
H: S(ubstitute) 40100 CR
40100 000 377 Δ [operator types 377 and a space]
40101 000 -    [operator types a hyphen]
40100 377 CR   [operator presses RETURN]
H:
```

T(est Memory)

The T(est Memory) command initiates the RAM memory test. The test references memory locations in the current radix. Error messages report the addresses of any bad memory locations.

V(iew)

The V(iew) command displays the contents of blocks of memory on the screen in the current radix and in ASCII. Non-printable characters appear as a graphics dot. Characters with the high order (parity) bit set appear in reverse video. The display begins at the first address specified, and continues through the second address. Starting and ending addresses should be separated with a comma.

If no starting or ending address is given, or if an address of zero is specified as the starting or ending address, the display begins at zero. V(iew) displays 128 bytes of data in octal if the current radix is octal, or 256 bytes in hexadecimal if the current radix is hexadecimal. Subsequent V(iew) commands which do not supply an argument display the next 128 or 256 bytes, depending on the setting of the current radix.

EXAMPLE 1: View the contents of memory locations 2280 through 2300 hex, where hexadecimal is the current radix.

```
H: V(iew)2280,2300  Ⓢ
2280  20 21 32 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F  !"#$%&'()*+,-./
2290  20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F  !"#$%&'()*+,-./
H:
```

EXAMPLE 2: View the contents of memory locations 0000 through 0128, where the current radix is octal. Then proceed to examine the next 128 bytes.

```
H: V(iew)  Ⓢ
000000  303 000 004 041 012 040 303 073  [C] 0 0 ! 0 [C] ;
000010  000 315 132 000 026 000 303 201  0 [M] Z 0 0 0 [C] 0
000020  000 315 132 000 032 303 244 001  0 [M] Z 0 0 [C] $ 0
.
.
.
000170  037 040 361 361 301 321 341 373  0 [q q A Q a {
H: V(iew)  Ⓢ
000200  311 052 033 040 043 042 033 040  [I] * 0 # " 0
etc.
```

EXAMPLE 3: View memory locations beginning with 2280 hex and continuing for 256 bytes, where hexadecimal is the current radix.

```
H: V(iew) 2280,  Ⓢ
2280  4A 4A 4A 4A ... 4A  JJJJJJJJJJJJJJ
.
.
.
2370  4A 4A 4A 4A ... 4A  JJJJJJJJJJJJJJ
```

PROGRAM EXECUTION CONTROL

When debugging an assembly language program, you can use MTR-90 commands to set breakpoints at, and continue execution from, various points in the program. Debugging can take place at any location above the lower 4K of memory. Be careful not to attempt to debug a program in the lower 4K of memory, as this area is occupied by MTR-90.

To set a breakpoint, use the S(ubstitute) command and put an HLT (hexadecimal 76, octal 166) instruction wherever you want the program to stop.

When your program reaches the breakpoint HLT instruction, it will return control to MTR-90 which will display an "H", then advance to a new line and display "H:". You can then use any MTR-90 command.

To continue your program, first restore the byte in the location into which you placed the breakpoint HLT. Since the computer had to execute the HLT instruction, the PC will point one beyond where you placed the HLT. To continue, decrement the PC value by one. Do this by entering the P(rogram Counter) command and pressing RETURN. When MTR-90 has displayed the current value of the PC, subtract one from that value, then enter the result into the PC.

You can alternatively use the G(o) command to start the program from whatever address you prefer, including from the location where you put the HLT.

Note that if the program which you are debugging uses keyboard interrupts, your program may contend with MTR-90 for console input. Your program should see every character input because the program receives the input via interrupts. But if the MTR-90 checks the keyboard for input after your program, the MTR-90 will not receive the input and no characters will be displayed on the screen. In other words, the fact that your keyboard input does not appear on the screen during program debugging using breakpoints does not mean that your program is at fault.

Appendix A

MTR-90 Listing

This appendix contains a listing of MTR-90. This program contains control routines for primitive keyboard input and screen output. MTR-90 needs available RAM in locations 2000H (040 000 octal) to 203FH (40 077 octal) and from 2150H (41 120 octal) to 2155 (41 125 octal). MTR-90 also needs 80 bytes of stack area in high memory.

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000.001

1 .DEBUG EQU 1
2

ASSEMBLE FOR DEBUG

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MTR89 IS A MODIFICATION OF MTR88 BY REX CHEN IN MAY, 1980.
MTR89 IS IDENTICAL TO THE MTR88 IN THAT ALL ENTRY POINTS TO
THE CURRENT ROUTINES REMAIN UNCHANGED AND ALL ROUTINES
REMAIN UNALTERED WITH THE FOLLOWING EXCEPTIONS:

- (1). TYPE SPACES TO DETERMINE BAUD RATE MESSAGE IS REMOVED.
- (2). THE BOOTSTRAP FOR THE Z-47 IS INSTALLED.
- (3). 15 SECONDS TIME OUT FOR Z-87, OR H-17 AND Z-47 IS INSERTED.
- (4). <DELETE> KEY SERVES AS AN ABORT-BOOT KEY.
- (5). ALLOWS BOOT FROM SELECT DEVICE AND UNIT.

MTR90 IS A MODIFICATION OF MTR89 TO ALLOW BOOTING FROM
THE H67, H37, AND 1 FUTURE DEVICE. ALSO THE H47 CODE WAS
CHANGED, AND HEXIDECIMAL ROUTINES WERE ADDED.
SEVERAL NEW "CONVENIENCE" COMMANDS WERE ADDED, THANKS TO
THE ADDITION OF THE EXTRA 2K SPACE.

MTR90-1 Employs a software fix for a hardware deficiency in disk
drives. It seems that a disk drive head may go into the negative
track area (-1, -2, ...) and not know it, so all disk drivers
have been modified to step the head in and then issuing a second
restore command. This can be taken care of in the hardware, but
people are opposed to adjusting hardware properly.

MTR88 IS AN ADAPTATION OF PAM/8 ORIGINALLY WRITTEN FOR THE
HEATH H8 COMPUTER BY J. G. LEITH IN 1976 AND MODIFIED BY
R. N. BORCHARDT IN 1979 FOR USE IN THE HEATH H88/H89
COMPUTERS.

MTR88 PROVIDES COMPATIBILITY WITH PAM/8 SUCH THAT ALL ROUTINES
HAVE RETAINED PREVIOUSLY DESCRIBED ENTRY POINTS AND ENTRY AND
EXIT CONDITIONS. ROUTINES WHICH ARE NOT APPLICABLE SUCH AS
THOSE PERTAINING TO THE FRONT PANEL DISPLAY HAVE BEEN DELETED.

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ST. JOSEPH, MI.

53 *** MTR88 - H88/H89 MONITOR.
 54 *
 55 * THIS PROGRAM RESIDES (IN ROM) IN THE LOW 2048 BYTES OF THE HEATH
 56 * H88/H89 COMPUTERS.

58 *** INTERRUPTS.
 59 *
 60 * MTR88 IS THE PRIMARY PROCESSOR FOR ALL INTERRUPTS.
 61 * THEY ARE PROCESSED AS FOLLOWS:
 62 *
 63 * RST USE
 64 *
 65 * 0 MASTER CLEAR. (NEVER USED FOR I/O OR RST)
 66 *
 67 * 1 CLOCK INTERRUPT. NORMALLY TAKEN BY MTR88,
 68 * SETTING BIT *UO-CLK* IN BYTE *MFLAG* ALLOWS
 69 * USER PROCESSING (VIA A JUMP THROUGH *UIVEC*
 70 * UPON ENTRY OF THE USER ROUTINE, THE STACK
 71 * CONTAINS:
 72 * (STACK+0) = RETURN ADDRESS (TO MTR88)
 73 * (STACK+2) = (STACKPTR+14)
 74 * (STACK+4) = (AF)
 75 * (STACK+6) = (BC)
 76 * (STACK+8) = (DE)
 77 * (STACK+10) = (HL)
 78 * (STACK+12) = (PC)
 79 * THE USER'S ROUTINE SHOULD RETURN TO MTR88 VIA
 80 * A *RET* WITHOUT ENABLING INTERRUPTS.
 81 *

82 * 2 SINGLE STEP INTERRUPTS RECEIVED WHEN IN
 83 * USER MODE CAUSES A JUMP THROUGH *UIVEC+3.
 84 * STACK UPON USER ROUTINE ENTRY:
 85 * (STACK+0) = (STACKPTR+12)
 86 * (STACK+2) = (AF)
 87 * (STACK+4) = (BC)
 88 * (STACK+6) = (DE)
 89 * (STACK+8) = (HL)
 90 * (STACK+10) = (PC)
 91 * THE USER'S ROUTINE SHOULD HANDLE IT'S OWN RETURN
 92 * FROM THE INTERRUPT.
 93 *
 94 *
 95 *
 96 * THE FOLLOWING INTERRUPTS ARE VECTORED DIRECTLY THROUGH *UIVEC*.
 97 * THE USER ROUTINE MUST HAVE SETUP A JUMP IN *UIVEC* BEFORE ANY
 98 * OF THESE INTERRUPTS MAY OCCUR.
 99 *
 100 * 3 I/O 3. CAUSES A DIRECT JUMP THROUGH *UIVEC+6
 101 *
 102 * 4 I/O 4. CAUSES A DIRECT JUMP THROUGH *UIVEC+9
 103 *
 104 * 5 I/O 5. CAUSES A DIRECT JUMP THROUGH *UIVEC+12
 105 *
 106 * 6 I/O 6. CAUSES A DIRECT JUMP THROUGH *UIVEC+15

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107 * 7 I/O 7. CAUSES A DIRECT JUMP THROUGH *UIVEC**18

109 ** ASSEMBLY CONSTANTS

000.331 111 MI.EXX EQU 331Q Z80 EXX INSTRUCTION
112
000.000 113 XTEXT MTR88 DEFINE MTR88 OLD EQUATES

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EQUATES FOR MTR88

IO PORTS

116X **
117X ***
118X ***
119X *
120X *
121X *
122X *
123X IP.PAD EQU 3600
124X OP.CTL EQU 3600
125X OP.DIG EQU 3600
126X OP.SEG EQU 3610
127X *
128X *
129X H88.CTL EQU 3620
130X H88B.CK EQU 00000010B
131X H88B.SS EQU 00000001B
132X *
133X H88.SW EQU 3620
134X H88S.AT EQU 10000000B
135X H88S.BR EQU 01000000B
136X H88S.M EQU 00100000B
137X H88S.OV EQU 00010000B
138X *
139X H88S.0 EQU 00001100B
140X *
141X H88S.4 EQU 00000011B
142X *

000.360
000.360
000.360
000.361
000.362
000.362
000.001
000.362
000.200
000.100
000.040
000.020
000.014
000.003
000.371
000.371
000.370
000.370

ALL REFERENCES TO THE H8 FRONT PANEL PORTS ARE TRAPPED BY THE
280 NMI OF THE H88/H89. OP.CTL WILL STILL PERFORM AS IN AN H8
IN RESPECT TO THE CLOCK AND SINGLE STEP CONTROL. FOR NOTE
INFORMATION SEE THE NMI ROUTINE.
PAD INPUT PORT
CONTROL OUTPUT PORT
DIGIT SELECT OUTPUT PORT
SEGMENT SELECT OUTPUT PORT
H88/H89 CONTROL PORT
H88/H89 PORT FOR THE CLOCK AND SINGLE STEP
2MS CLOCK ENABLE/DISABLE
SINGLE STEP ENABLE/DISABLE
8 POSITION DIP SWITCH
AUTO BOOT SWITCH
BAUD RATE SWITCH
MEMORY TEST/NORMAL OPERATION SWITCH
-0, BOOT FROM DEVICE AT 174-1770
-1, BOOT FROM DEVICE AT 170-1730
DEVICE AT 170-1730: 0 = 237, 1 = 247
2 = 267, 3 = UNKNOWN
DEVICE AT 174-1770: 0 = H17, 1 = 247
2 = 267, 3 = UNKNOWN

CASSETTE PORTS

ASCII CHARACTERS

151X **
152X
153X A.SYN EQU 0260
154X A.STX EQU 0020
155X A.BEL EQU 0070
156X A.BKS EQU 0100
157X A.LF EQU 0120
158X A.CR EQU 0150
159X A.ESC EQU 0330
160X A.DEL EQU 1770

SYNC CHARACTER
STX CHARACTER
BELL CHARACTER
BACKSPACE CHARACTER
LINE FEED CHARACTER
CARRIAGE RETURN CHARACTER
ESCAPE CHARACTER
DELETE OR RUBOUT CHARACTER

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162X **	FRONT PANEL HARDWARE CONTROL BITS
163X	
000.020	164X CB.SSI EQU 00010000B SINGLE STEP INTERRUPT
000.040	165X CB.MTL EQU 00100000B MONITOR LIGHT
000.100	166X CB.CLI EQU 01000000B CLOCK INTERRUPT ENABLE
000.200	167X CB.SPK EQU 10000000B SPEAKER ENABLE

169X **	DISPLAY MODE FLAGS (IN *DSPMOD*)
170X	
000.000	171X DM.MR EQU 0 MEMORY READ
000.001	172X DM.MW EQU 1 MEMORY WRITE
000.002	173X DM.RR EQU 2 REGISTER READ
000.003	174X DM.RW EQU 3 REGISTER WRITE

176X **	MACHINE INSTRUCTIONS
177X	
000.166	178X MI.HLT EQU 0110110B HALT
000.311	179X MI.RET EQU 11001001B RETURN
000.333	180X MI.IN EQU 11011011B INPUT
000.323	181X MI.OUT EQU 11010011B OUTPUT
000.072	182X MI.LDA EQU 00111010B LOA
000.346	183X MI.ANI EQU 11100110B ANI
000.021	184X MI.LXID EQU 00010001B LXI D
000.303	185X MI.JMP EQU 11000011B JMP
000.335	186X MI.LDXA EQU 11011101B LD IX, (BYTE A)
000.041	187X MI.LDXB EQU 00100001B LD IX, (BYTE B)
000.375	188X MI.LDYA EQU 11111101B LD IY, (BYTE A)
000.041	189X MI.LDYB EQU 00100001B LD IY, (BYTE B)
000.010	190X MI.EXAF EQU 00001000B EX AF,AF
000.335	191X MI.JIXA EQU 11011101B JP (IX) (BYTE A)
000.351	192X MI.JIXB EQU 11010011B JP (IX) (BYTE B)
000.375	193X MI.JIYA EQU 11111101B JP (IY) (BYTE A)
000.351	194X MI.JIYB EQU 11101001B JP (IY) (BYTE B)

196X ** USER OPTION BITS.

197X * THESE BITS ARE SET IN CELL .HFLAG.

198X *	
199X	
000.200	200X U0.HLT EQU 10000000B DISABLE HALT PROCESSING
000.100	201X U0.NFR EQU CB.CLI NO REFRESH FRONT PANEL
000.002	202X U0.ODU EQU 00000010B DISABLE DISPLAY UPDATE
000.001	203X U0.CLK EQU 00000001B ALLOW PRIVATE INTERRUPT PROCESSING
000.000	204 XTEXT H17DEF EQUATES FOR H17 800T ROM

H17

H17 CONTROL INFORMATION.

206X **	H17 CONTROL INFORMATION.	206X **	H17 CONTROL INFORMATION.
207X		207X	
208X DP.DC EQU 07FH	DISK CONTROL PORT	208X DP.DC EQU 07FH	DISK CONTROL PORT
209X		209X	
210X DF.HD EQU 0000001B	HOLE DETECT	210X DF.HD EQU 0000001B	HOLE DETECT
211X DF.YO EQU 0000010B	TRACK 0 DETECT	211X DF.YO EQU 0000010B	TRACK 0 DETECT
212X DF.WP EQU 0000100B	WRITE PROTECT	212X DF.WP EQU 0000100B	WRITE PROTECT
213X DF.SD EQU 0000100B	SYNC DETECT	213X DF.SD EQU 0000100B	SYNC DETECT
214X		214X	
215X DF.WG EQU 00000001B	WRITE GATE ENABLE	215X DF.WG EQU 00000001B	WRITE GATE ENABLE
216X DF.DS0 EQU 0000010B	DRIVE SELECT 0	216X DF.DS0 EQU 0000010B	DRIVE SELECT 0
217X DF.DS1 EQU 0000100B	DRIVE SELECT 1	217X DF.DS1 EQU 0000100B	DRIVE SELECT 1
218X DF.DS2 EQU 0001000B	DRIVE SELECT 2	218X DF.DS2 EQU 0001000B	DRIVE SELECT 2
219X DF.M0 EQU 0001000B	MOTOR ON (BOTH DRIVES)	219X DF.M0 EQU 0001000B	MOTOR ON (BOTH DRIVES)
220X DF.O1 EQU 0010000B	DIRECTION (0-OUT)	220X DF.O1 EQU 0010000B	DIRECTION (0-OUT)
221X DF.ST EQU 0100000B	STEP COMMAND (ACTIVE HIGH)	221X DF.ST EQU 0100000B	STEP COMMAND (ACTIVE HIGH)
222X DF.WR EQU 1000000B	WRITE ENABLE RAM	222X DF.WR EQU 1000000B	WRITE ENABLE RAM
223X		223X	
224X		224X	
225X		225X	
226X **	DISK UART PORTS AND CONTROL FLAGS.	226X **	DISK UART PORTS AND CONTROL FLAGS.
227X		227X	
228X UP.DP EQU 07CH	DATA PORT	228X UP.DP EQU 07CH	DATA PORT
229X UP.FC EQU 07DH	FILL CHARACTER	229X UP.FC EQU 07DH	FILL CHARACTER
230X UP.ST EQU 07DH	STATUS FLAGS	230X UP.ST EQU 07DH	STATUS FLAGS
231X UP.SC EQU 07EH	SYN CHARACTER (OUTPUT)	231X UP.SC EQU 07EH	SYN CHARACTER (OUTPUT)
232X UP.SR EQU 07EH	SYNC RESET (INPUT)	232X UP.SR EQU 07EH	SYNC RESET (INPUT)
233X		233X	
234X UF.RDA EQU 0000001B	RECEIVE DATA AVAILABLE	234X UF.RDA EQU 0000001B	RECEIVE DATA AVAILABLE
235X UF.ROR EQU 0000010B	RECEIVER OVERRUN	235X UF.ROR EQU 0000010B	RECEIVER OVERRUN
236X UF.RPE EQU 0000100B	RECEIVER PARITY ERROR	236X UF.RPE EQU 0000100B	RECEIVER PARITY ERROR
237X UF.FCT EQU 0100000B	FILL CHAR TRANSMITTED	237X UF.FCT EQU 0100000B	FILL CHAR TRANSMITTED
238X UF.TBM EQU 1000000B	TRANSMITTER BUFFER EMPTY	238X UF.TBM EQU 1000000B	TRANSMITTER BUFFER EMPTY
239X		239X	
240X		240X	
241X		241X	
242X **	CHARACTER DEFINITIONS.	242X **	CHARACTER DEFINITIONS.
243X		243X	
244X C.DSYN EQU 0FDH	PREFIX SYNC CHARACTER	244X C.DSYN EQU 0FDH	PREFIX SYNC CHARACTER
245	XTEXT H37DEF	245	XTEXT H37DEF
246X **	H37DEF - H37 DISK CONTROLLER DEFINITIONS	246X **	H37DEF - H37 DISK CONTROLLER DEFINITIONS
247X		247X	
248X DK.PORT EQU 170Q	BASE UART PORT	248X DK.PORT EQU 170Q	BASE UART PORT
249X		249X	
250X FD.STAT EQU DK.PORT+2	STATUS PORT	250X FD.STAT EQU DK.PORT+2	STATUS PORT
251X FD.CMD EQU DK.PORT+2	COMMAND PORT	251X FD.CMD EQU DK.PORT+2	COMMAND PORT
252X FD.TRK EQU DK.PORT+3	TRACK REGISTER	252X FD.TRK EQU DK.PORT+3	TRACK REGISTER
253X FD.SEC EQU DK.PORT+2	SECTOR REGISTER	253X FD.SEC EQU DK.PORT+2	SECTOR REGISTER
254X FD.DAT EQU DK.PORT+3	DATA PORT	254X FD.DAT EQU DK.PORT+3	DATA PORT
255X DK.COM EQU DK.PORT	CONTROL PORT	255X DK.COM EQU DK.PORT	CONTROL PORT
256X DK.INT EQU DK.PORT+1	INTERFACE CONTROL	256X DK.INT EQU DK.PORT+1	INTERFACE CONTROL
257X		257X	
258X **	COMMANDS SENT TO FD.CMD	258X **	COMMANDS SENT TO FD.CMD
259X		259X	
260X FDC.RST EQU 0000000B	RESTORE	260X FDC.RST EQU 0000000B	RESTORE
261X FDC.SEK EQU 0001000B	SEEK TRACK IN FD.TRK	261X FDC.SEK EQU 0001000B	SEEK TRACK IN FD.TRK

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 EQUATES FOR MTR88 10:40:30 17-FEB-82

000.040	262X FDC.STP EQU	00100000B	STEP IN SAME DIR AS LAST
000.100	263X FDC.STI EQU	01000000B	STEP IN
000.140	264X FDC.STO EQU	01100000B	STEP OUT
000.200	265X FDC.RDS EQU	10000000B	READ SECTOR
000.240	266X FDC.WTS EQU	10100000B	WRITE SECTOR
000.300	269X FDC.RDA EQU	11000000B	READ ADDRESS
000.340	270X FDC.RDI EQU	11100000B	READ TRACK
000.360	271X FDC.WTI EQU	11110000B	WRITE TRACK
000.320	272X FDC.FI EQU	11010000B	FORCE INTERRUPT
000.020	274X **	OPTIONS FOR FDC.RST THRU FDC.STO	
000.010	275X FDC.UTR EQU	00010000B	UPDATE TRACK REGISTER
000.004	278X FDC.HLB EQU	00001000B	LOAD HEAD AT BEGINING
000.000	279X FDC.VRF EQU	00000100B	VERIFY DESTINATION
000.000	280X		
000.001	281X FDC.S6 EQU	00000000B	STEP 6 MS
000.002	282X FDC.S12 EQU	00000001B	STEP 12 MS
000.003	283X FDC.S20 EQU	00000010B	STEP 20 MS
000.001	284X FDC.S30 EQU	00000011B	STEP 30 MS
000.020	285X **	OPTIONS FOR FDC.RDS THRU FDC.WTI	
000.010	287X FDC.MRF EQU	00010000B	MULTY RECORD FLAG
000.004	289X FDC.SLF EQU	00001000B	SECTOR LENGTH SHIFT RIGHT
000.002	290X FDC.DLF EQU	00000100B	15 (30) MS DELAY
000.001	291X FDC.SSI EQU	00000010B	SELECT SIDE 1
000.000	292X FDC.DDM EQU	00000001B	DELETED DATA MARK
000.020	293X **	STATUS BIT DEFINITIONS	
000.100	294X		
000.040	295X FDS.NRD EQU	10000000B	NOT READY
000.040	297X FDS.WPV EQU	01000000B	WRITE PROTECT
000.040	298X FDS.HLD EQU	00100000B	HEAD IS LOADED
000.040	299X FDS.RTE EQU	00100000B	RECORD TYPE
000.020	300X FDS.MTF EQU	00100000B	WRITE FAULT
000.020	301X FDS.SEK EQU	00010000B	SEEK ERROR
000.010	302X FDS.RNF EQU	00010000B	RECORD NOT FOUND
000.004	303X FDS.CRC EQU	00001000B	CRC ERROR
000.004	304X FDS.TKO EQU	00000100B	OVER TRACK ZERO
000.002	305X FDS.LDT EQU	00000100B	LOST DATA
000.002	306X FDS.IND EQU	00000010B	INDEXZ PULSE
000.001	307X FDS.DRQ EQU	00000010B	DATA REQUEST
000.001	308X FDS.BSY EQU	00000001B	BUSY
000.001	309X *	BITS SET IN DK.CON	
000.002	310X		
000.004	312X CON.EI EQU	00000001B	ENABLE INT-REQ
000.010	313X CON.DRQ EQU	00000010B	ENABLE DRQ INTERRUPT
000.020	314X CON.MFM EQU	00000100B	SET MFM RECORDING
000.040	315X CON.MO EQU	00001000B	ALL MOTORS ON
000.040	316X CON.DSO EQU	00010000B	DRIVE 0
000.040	317X CON.DSI EQU	00100000B	DRIVE 1

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EQUATES FOR MTR88 10:40:31 17-FEB-82

000.100 318X CON.DS2 EQU 010000008 DRIVE 2
000.200 319X CON.DS3 EQU 100000008 DRIVE 3
320X

321X
322X * Bits set to select alternate registers

323X
000.000 324X CON.CD EQU 000000008 SELECT COMMAND/DATA
000.001 325X CON.ST EQU 000000018 SELECT SECTOR/TRACK
000.000 326 XTEXT Z47DEF DEFINE Z47 EQUATES

328X ** H47DEF - H47 Constant Definitions
329X *

331X * Z80 Instructions

332X
242.355 333X M.INI EQU 101000108*256+111011018 INI Instruction
243.355 334X M.OUTI EQU 101000118*256+111011018 OUTI Instructions

336X ** DISK INTERFACE CONSTANTS

337X *
338X
000.170 339X D.STA EQU 170Q INTERFACE STATUS PORT
000.171 340X D.DAT EQU D.STA+1 INTERFACE DATA PORT
341X
000.001 342X S.ERR EQU 000000018 ERROR BIT
000.040 343X S.DON EQU 001000008 DONE
000.100 344X S.IEN EQU 010000008 INTERRUPT ENABLE
000.200 345X S.DIR EQU 100000008 DATA TRANSFER REQUEST
346X
000.002 347X S.SW0 EQU 000000108 DIP SWITCH 0
000.004 348X S.SW1 EQU 000001008 DIP SWITCH 1
000.010 349X S.SW2 EQU 000010008 DIP SWITCH 2
000.020 350X S.SW3 EQU 000100008 DIP SWITCH 3
351X
000.002 352X W.RES EQU 000000108 RESET COMMAND

354X ** STATUS BYTE FLAGS

355X *
356X
000.200 357X SB.UNR EQU 100000008 UNIT NOT READY
000.100 358X SB.WPD EQU 010000008 WRITE PROTECTED DRIVE
000.040 359X SB.DLD EQU 001000008 DELETED DATA
000.020 360X SB.NRF EQU 000100008 NO RECORD FOUND
000.010 361X SB.CRC EQU 000010008 CRC ERROR

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EQUATES FOR MTR88 10:40:32 17-FEB-82

000.004	362X SB.LTD EQU	00000100B	LATE DATA
000.002	363X SB.ILC EQU	00000010B	ILLEGAL COMMAND
000.001	364X SB.BTD EQU	00000001B	BAD TRACK OVERFLOW

AUXILIARY STATUS BYTE FLAGS

000.100	366X **	369X AS.00D EQU	01000000B	TRACK 0 DOUBLE DENSITY
000.040	367X *	370X AS.10D EQU	00100000B	TRACK 1-76 DOUBLE DENSITY
000.020		371X AS.S1A EQU	00010000B	SIDE 1 AVAILABLE
000.003		372X AS.SLM EQU	00000011B	SECTOR LENGTH MASK

DISK COMMANDS

000.000	374X **	377X	DD.BOOT DS	0	BOOT
000.000	375X *	378X	DD.RST DS	1	READ CONTROLLER STATUS
000.001		379X	DD.RAS DS	1	READ AUX. STATUS
000.002		380X	DD.LSC DS	1	LOAD SECTOR COUNT
000.003		381X	DD.RAD DS	1	READ ADDR. OF LAST SECTOR ACCESSED
000.004		382X	DD.REA DS	1	READ SECTORS
000.005		383X	DD.WRI DS	1	WRITE SECTORS
000.006		384X	DD.WR0 DS	1	READ SECTORS BUFFERED
000.007		385X	DD.WR1 DS	1	WRITE SECTORS & DELETE
000.010		386X	DD.WR2 DS	1	WRITE SECTORS BUFFERED & DELETE
000.011		387X	DD.WR3 DS	1	COPY
000.012		388X	DD.WR4 DS	1	FORMAT IBM SD
000.013		389X	DD.WR5 DS	1	FORMAT SD
000.014		390X	DD.WR6 DS	1	FORMAT IBM DD
000.015		391X	DD.WR7 DS	1	FORMAT DD
000.016		392X	DD.WR8 DS	1	READ READY
000.017		393X	DD.WR9 DS	1	
000.020		394X	DD.WR0 DS	1	

Special De-Bug functions

000.020	396X **	399X	DD.SPF0 DS	1	SPECIAL FUNCTION 0
000.021	397X *	400X	DD.SPF1 DS	1	SPECIAL FUNCTION 1
000.022		401X	DD.SPF2 DS	1	SPECIAL FUNCTION 2
000.023		402X	DD.SPF3 DS	1	SPECIAL FUNCTION 3
000.024		403X	DD.SPF4 DS	1	SPECIAL FUNCTION 4
000.025		404X	DD.SPF5 DS	1	SPECIAL FUNCTION 5

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EQUATES FOR MTR88

407X ** Special Heath Functions

```

408X *
409X
000.200 410X DD.SDC DS 1 080H
000.200 411X DD.SDC DS 1
000.201 412X DD.SF DS 1
000.202 413X DD.DS DS 1
000.203 414X DD.RDL DS 1
000.204 415X DD.WTL DS 1
000.205 416X DD.RDL DS 1
000.206 417X DD.WTL DS 1
000.207 418X DD.WTL DS 1
000.210 419X DD.WDLB DS 1

```

SET DRIVE CHARACTERISTIC
SEEK TO TRACK
DISK STATUS
READ LOGICAL
WRITE LOGICAL
READ BUFFERED LOGICAL
WRITE BUFFERED LOGICAL
WRITE DELETED DATA LOGICAL
WRITE BUFFERED DELETED DATA LOGICAL

421X ** USEFUL FLAGS

```

422X *
423X
000.000 424X UNT.0 EQU 00000000B UNIT 0
000.040 425X UNT.1 EQU 00100000B UNIT 1
000.100 426X UNT.2 EQU 01000000B UNIT 2
000.140 427X UNT.3 EQU 01100000B UNIT 3

```

Unit mask

```

000.140 429X UNT.M EQU 01100000B
430X
431X
432X
000.000 433X SID.0 EQU 00000000B Side: 0
000.200 434X SID.1 EQU 10000000B Side: 1
435X
000.200 436X SID.M EQU 10000000B Side Mask
437X
438X

```

Track Mask

```

000.037 439X SEC.M EQU 00011111B
440X
441X
442X

```

Maximum Sector Size

```

004.000 443X SSIZ.M EQU 1024
444X
445X

```

SECTOR SIZE = 256 BYTES
SECTOR SIZE

```

447X *C.256 EQU 256
448X *C.128 EQU 128
449X *C.26 EQU 26

```

H67 DEFINITIONS

```

000.211 450 XTEXT H67DEF

```

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 H67 Disk Controller Definitions 10:40:35 17-FEB-82

453X ** H67 Disk Controller Definitions
 454X *

456X **	Register addresses	457X *	458X	459X BASE	EQU	1700	Controller base address
000.170	460X						
000.000	461X RI-DAT	EQU	0				Data In/Out (Read/Write)
000.001	462X RI-COM	EQU	1				Control (Write Only)
000.001	463X RI-BST	EQU	1				Bus Status (Read Only)

465X * Control Register Definition

000.100	466X						
000.090	467X BC-SEL	EQU	01000000B				Select and data bit 0
000.020	468X BC-IE	EQU	00100000B				Interrupt Enable
000.002	469X BC-RST	EQU	00010000B				Reset
000.002	470X BC-EDT	EQU	00000010B				Enable Data

472X * Bus Status Register Definition

000.200	473X						
000.100	474X BS-REQ	EQU	10000000B				Data Transfer Request
000.000	475X BS-DTD	EQU	01000000B				Data Transfer Direction
000.100	476X BS-IN	EQU	00000000B				Data to Host
000.040	477X BS-OUT	EQU	01000000B				Data to Controller
000.020	478X BS-LMB	EQU	00100000B				Last byte in data/command string
000.000	479X BS-MTY	EQU	00010000B				Message type
000.010	480X BS-DAT	EQU	00000000B				Data
000.020	481X BS-COM	EQU	00010000B				Command
000.010	482X BS-BSY	EQU	00001000B				Busy
000.004	483X BS-INT	EQU	00000100B				Interrupt Pending
000.002	484X BS-PE	EQU	00000010B				Parity Error
000.001	485X BS-HIO	EQU	00000001B				Hardware Identification

487X * Status Byte Definitions

000.140	488X						
000.034	489X ST-LUN	EQU	01100000B				Logical Unit
000.002	490X ST-SPR	EQU	00011000B				Spare
000.001	491X ST-EKR	EQU	00000010B				Error
000.001	492X ST-PER	EQU	00000001B				Parity Error

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H67 Disk Controller Definitions

494X ** Commands

495X *

496X

497X CLASSM EQU 111000008 Class Mask

498X

499X CLASS0 EQU 000000008 Class 0

500X CLASS1 EQU 001000008 Class 1

501X CLASS6 EQU 110000008 Class 6

502X

503X OPC00H EQU 000111118 Op-code Mask

504X LUNH EQU 011000008 Logical Unit Mask

505X LSA.2 EQU 000111118 Logical Sector Address (2)

507X * Class 0 Commands

508X

509X D.TDR EQU CLASS0+0 Test drive ready

510X D.REC EQU CLASS0+1 Recalibrate drive

511X D.RSY EQU CLASS0+2 Request Syndrome

512X D.RSE EQU CLASS0+3 Request Sense

513X D.FOR EQU CLASS0+4 Format Drive

514X D.CTF EQU CLASS0+5 Check track format

515X D.FI EQU CLASS0+6 Format track

516X D.FBS EQU CLASS0+7 Format bad sector

517X D.REA EQU CLASS0+8 Read

518X D.WPS EQU CLASS0+9 Write protect the sector

519X D.WRI EQU CLASS0+10 Write

520X D.SEK EQU CLASS0+11 Seek

522X * Class 1 Commands

523X

524X D.CPB EQU CLASS1+0 Copy block

526X * Class 6 Commands

527X

528X D.FFD EQU CLASS6+0 Format floppy disk

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Hd7 Disk Controller Definitions 10:40:37 17-FEB-82

530X * Type 0 error codes (Drive error Codes)

531X	EQU	0	No status
000.000	532X T0.MST	EQU	1
000.001	533X T0.MIS	EQU	2
000.002	534X T0.NSC	EQU	3
000.003	535X T0.WFT	EQU	4
000.004	536X T0.DNR	EQU	5
000.005	537X T0.DNS	EQU	6
000.006	538X T0.NTO	EQU	7
000.007	539X T0.MDS	EQU	

541X * Type 1 error codes (data error codes)

542X	EQU	0	ID Read Error
000.000	543X T1.ID	EQU	1
000.001	544X T1.UDE	EQU	2
000.002	545X T1.IDMF	EQU	3
000.003	546X T1.DNMF	EQU	4
000.004	547X T1.RNF	EQU	5
000.005	548X T1.SKE	EQU	6
000.006	549X T1.DYE	EQU	7
000.007	550X T1.WP	EQU	8
000.010	551X T1.CDE	EQU	9
000.011	552X T1.BBF	EQU	10
000.012	553X T1.FE	EQU	

555X * Type 2 Error Codes (Command error codes)

556X	EQU	0	Illegal Command
000.000	557X T2.ILC	EQU	1
000.001	558X T2.IDA	EQU	2
000.002	559X T2.IFN	EQU	
000.211	560	XTEXT	HDSEQU

562X ** HDOS SYSTEM EQUIVALENCES.

563X *			
564X			
024.000	565X S.GRT0	EQU	24000A
025.000	566X S.GRT1	EQU	25000A
026.000	567X S.GRT2	EQU	26000A
030.000	568X		
	569X ROMBOOT	EQU	30000A
040.100	570X		
	571X	ORG	40100A
	572X		
040.100	573X	DS	8
040.110	574X D.CON	DS	16
040.130	575X SY00	EQU	*
	576X D.VEC	DS	24*3

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H67 Disk Controller Definitions			ESINT	10:40:54 17-FEB-82	
040.344	628X S.8AUD DS 2		[0-14]	H8-4 BAUD RATE, =0 IF H8-5	
	629X * 630X		[15]	-1 IF 2 STOP BITS	
	631X **	TABLE ADDRESS WORDS			
	632X				
040.346	633X S.DLINK DS 2			ADDRESS OF DATA IN HDOS CODE	
040.350	634X S.OFMA DS 2			FMA OVERLAY TABLE	
040.352	635X S.CFMA DS 2			FMA CHANNEL TABLE	
040.354	636X S.DFMA DS 2			FMA DEVICE TABLE	
040.356	637X S.RFMA DS 2			FMA RESIDENT HDOS CODE	
	638X				
	639X **	DEVICE DRIVER DELAYED LOAD FLAGS			
	640X				
040.360	641X S.DDLDA DS 2			DRIVER LOAD ADDRESS (HIGH BYTE=0 IF NO LOAD PENDING)	
040.362	642X S.DDLEN DS 2			CODE LENGTH IN BYTES	
040.364	643X S.DDGRP DS 1			GROUP NUMBER FOR DRIVER	
040.365	644X DS 1			HOLD PLACE	
	645X *S.DDSEC DS 2			SECTOR NUMBER FOR DRIVER (* OBSOLETE ! *)	
040.366	646X S.DDDTA DS 2			DEVICE'S ADDRESS IN DEVLST +DEV.RES	
040.370	647X S.DDOPC DS 1			OPEN OP CODE PENDING	
	648X				
	649X **	OVERLAY MANAGEMENT FLAGS			
	650X				
000.001	651X OVL.IN EQU 00000001B			IN MEMORY	
000.002	652X OVL.RES EQU 00000010B			PERMANENTLY RESIDENT	
000.014	653X OVL.NUM EQU 0001100B			OVERLAY NUMBER MASK	
000.200	654X OVL.UCS EQU 10000000B			USER CODE SHAPPED FOR OVERLAY	
	655X				
040.371	656X S.OVLFL DS 1			OVERLAY FLAG	
040.372	657X S.UCSF DS 2			FMA SHAPPED USER CODE	
040.374	658X S.UCSL DS 2			LENGTH SHAPPED USER CODE	
040.376	659X S.OVLS DS 2			SIZE OF OVERLAY CODE	
041.000	660X S.OVLE DS 2			ENTRY POINT OF OVERLAY CODE	
	661X				
041.002	662X S.SSN DS 2			SWAP AREA SECTOR NUMBER	
041.004	663X S.OSN DS 2			OVERLAY SECTOR NUMBER	
	664X				
	665X *	SYSCALL PROCESSING WORK AREAS			
	666X				
041.006	667X S.CACC DS 1			(ACC) UPON SYSCALL	
041.007	668X S.CODE DS 1			SYSCALL INDEX IN PROGRESS	
	669X				
	670X *	JUMPS TO ROUTINES IN RESIDENT HDOS CODE			
	671X				
041.010	672X S.JUMPS DS 0			START OF JUMP VECTORS	
041.010	673X S.SDD DS 3			JUMP TO STAND-IN DEVICE DRIVER	
041.013	674X S.FASER DS 3			JUMP TO FATERR (FATAL SYSTEM ERROR)	
041.016	675X S.DIREA DS 3			JUMP TO DIREAD (DISK FILE READ)	
041.021	676X S.FCI DS 3			JUMP TO FCI (FETCH CHANNEL INFO)	
041.024	677X S.SCI DS 3			JUMP TO SCI (STORE CHANNEL INFO)	
041.027	678X S.GUP DS 3			JUMP TO GUP (GET UNIT POINTER)	
	679X				
041.032	680X S.MOUNT DS 1			<0 IF THE SYSTEM DISK IS MOUNTED	
041.033	681X S.DCS DS 1			DEFAULT CLUSTER SIZE-1	
	682X				
041.034	683X S.BOOTF DS 1			BOOT FLAGS	

H67 Disk Controller Definitions

ESINT

000.001	684X	BOOT.P	DS	000000018	EXECUTE PROLOGUE UPON BOOTUP	/2.1b/
000.002	685X	BOOT.SY	DS	000000108	SY: Device Driver loaded	
	686X					
	687X	*			STACK VALUE SAVED FOR OVERLAY SYSCALLS	
	688X					
041.035	689X	S.OVSYSK	DS	2	VALUE OF SP UPON SYSCALLS USING OVERLAY	
	690X					
041.037	691X	DS	1		RESERVED	
	693X	**			ACTIVE I/O AREA.	
	694X	*				
	695X	*			THE AIO.XXX AREA CONTAINS INFORMATION ABOUT THE I/O OPERATION	
	696X	*			CURRENTLY BEING PERFORMED. THE INFORMATION IS OBTAINED FROM	
	697X	*			THE CHANNEL TABLE, AND WILL BE RESTORED THERE WHEN DONE.	
	698X	*				
	699X	*			NORMALLY, THE AIO.XXX INFORMATION WOULD BE OBTAINED DIRECTLY	
	700X	*			FROM VARIOUS SYSTEM TABLES VIA POINTER REGISTERS. SINCE THE	
	701X	*			8080 HAS NO GOOD INDEXED ADDRESSING, THE DATA IS MANUALLY	
	702X	*			COPIED INTO THE AIO.XXX CELLS BEFORE PROCESSING, AND	
	703X	*			BACKDATED AFTER PROCESSING.	
	704X					
	705X	AIO.VEC	DS	3	JUMP INSTRUCTION	
041.040	706X	AIO.OOA	DS	**2	DEVICE DRIVER ADDRESS	
041.041	707X	AIO.FLG	DS	1	FLAG BYTE	
041.043	708X	AIO.GRT	DS	2	ADDRESS OF GROUP RESERV TABLE	
041.044	709X	AIO.SPG	DS	1	SECTORS PER GROUP	
041.046	710X	AIO.CGN	DS	1	CURRENT GROUP NUMBER	
041.047	711X	AIO.CSI	DS	1	CURRENT SECTOR INDEX	
041.050	712X	AIO.LGN	DS	1	LAST GROUP NUMBER	
041.051	713X	AIO.LSI	DS	1	LAST SECTOR INDEX	
041.052	714X	AIO.DTA	DS	2	DEVICE TABLE ADDRESS	
041.053	715X	AIO.DES	DS	2	DIRECTORY SECTOR	
041.055	716X	AIO.DEV	DS	2	DEVICE CODE	
041.057	717X	AIO.UNI	DS	1	UNIT NUMBER (0-9)	
041.061	718X					
041.062	719X	AIO.DIR	DS	DIRELEN	DIRECTORY ENTRY	
	720X					
041.111	721X	AIO.CNT	DS	1	SECTOR COUNT	
041.112	722X	AIO.EOM	DS	1	END OF MEDIA FLAG	
041.113	723X	AIO.EOF	DS	1	END OF FILE FLAG	
041.114	724X	AIO.TFP	DS	2	TEMP FILE POINTERS	
041.116	725X	AIO.CHA	DS	2	ADDRESS OF CHANNEL BLOCK (IOC.DDA)	
	727X	S.8DA	DS	1	Boot Device address (Setup by ROM) /80.09.gc/	
041.120	728X	S.SCR	DS	2	SYSTEM SCRATCH AREA ADDRESS	
041.121	729X	DS	3			
041.123	730X	ERNZ	DS	**41126A		
000.000	731X	S.OSI	DS	1	Operating System ID	/2.1b/
041.126	732X	S.OSO	DS	1	Operating System Occurance	/2.1b/
041.127	733X	S.OSZ	DS	3	Operating System Sector Zero	/2.1b/
041.130						

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041.133 734 XTEXT MISC MISCELLANEOUS EQUATES FOR H17 BOOT ROM

737X ** MISCELLANEOUS EQUATES FROM H17 BOOT ROM.
 738X * REFER TO H17 BOOT ROM IF MORE INFORMATION DESIRED
 739X
 740X WHD EQU 36235A WAIT FOR HOLE ROUTINE ENTRY POINT
 741X MNH EQU 36271A WAIT FOR NO HOLE ROUTINE ENTRY POINT
 742X
 000.130 743X BOOTAL EQU 130A NUMBER OF RAM TO CLEAR
 037.132 744X BOOTA EQU 37132A RAM CLEAR START LOCATION
 030.252 745X \$MOVE EQU 30252A MOVE DATA ROUTINE
 000.037 746X D.RAML EQU 37Q
 031.212 747X \$ZERO EQU 31212A ZERO RAM ROUTINE
 040.037 748X .UIVEC EQU 40037A USER INTERRUPT VECTOR
 034.031 749X CLOCK17 EQU 34031A 217 TIMER INTERRUPT HANDLER LOCATION
 033.366 750X R-ABORT EQU 33366A RESET 217 ROUTINE LOCATION
 034.077 751X R-READ EQU 34077A READ 217 ROUTINE LOCATION
 040.206 752X D.SDP EQU 40206A SET DEVICE PARAMETER RAM LOCATION
 040.166 753X D.SDT EQU 40166A SEEK DESIRED TRACK
 040.240 754X D.IT EQU 40240A TARGET TRACK BYTE
 036.073 755X SDP3 EQU 36073A SET DEVICE PARAMETER ENTRY
 034.027 756X EIXIT EQU 34027A EI/RET LOCATION
 000.012 757X ERPTCNT EQU 12Q ERROR COUNT
 040.264 758X D.OECNT EQU 40264A
 041.133 759 XTEXT U8251 DEFINE 8251 USART BITS

MTR90-1 - H/2-89 MONITOR #09.02.01.
8251 USART BIT DEFINITIONS.

762X ** 8251 USART BIT DEFINITIONS.

763X *

764X

765X ** PORT ADDRESSES

766X

000.000 767X UDR EQU 0 DATA REGISTER IS EVEN

000.001 768X USR EQU 1 STATUS REGISTER IS NEXT

000.372 770X SC.UART EQU 3720 CONSOLE USART ADDRESS (IFF 8251)

771X

772X

773X ** MODE INSTRUCTION CONTROL BITS.

774X

000.100 775X UMI.LB EQU 01000000B 1 STOP BIT

000.200 776X UMI.HB EQU 10000000B 1 1/2 STOP BITS

000.300 777X UMI.2B EQU 11000000B 2 STOP BITS

000.040 778X UMI.PE EQU 00100000B EVEN PARITY

000.020 779X UMI.PA EQU 00010000B USE PARITY

000.000 780X UMI.L5 EQU 00000000B 5 BIT CHARACTERS

000.004 781X UMI.L6 EQU 00000100B 6 BIT CHARACTERS

000.010 782X UMI.L7 EQU 00001000B 7 BIT CHARACTERS

000.014 783X UMI.L8 EQU 00001100B 8 BIT CHARACTERS

000.001 784X UMI.LX EQU 00000001B CLOCK X 1

000.002 785X UMI.L6X EQU 00000010B CLOCK X 16

000.003 786X UMI.64X EQU 00000011B CLOCK X 64

787X

788X ** COMMAND INSTRUCTION BITS.

789X

000.100 790X UCI.IR EQU 01000000B INTERNAL RESET

000.040 791X UCI.R0 EQU 00100000B READER-ON CONTROL FLAG

000.020 792X UCI.ER EQU 00010000B ERROR RESET

000.004 793X UCI.RE EQU 00000100B RECEIVE ENABLE

000.002 794X UCI.IE EQU 00000010B ENABLE INTERRUPTS FLAG

000.001 795X UCI.TE EQU 00000001B TRANSMIT ENABLE

796X

797X ** STATUS READ COMMAND BITS.

798X

000.040 799X USR.FE EQU 00100000B FRAMING ERROR

000.020 800X USR.DE EQU 00010000B OVERRUN ERROR

000.010 801X USR.PE EQU 00001000B PARITY ERROR

000.004 802X USR.IXE EQU 00000100B TRANSMITTER EMPTY

000.002 803X USR.RXR EQU 00000010B RECEIVER READY

000.001 804X USR.TXR EQU 00000001B TRANSMITTER READY

041.133 805 XTXT U8250 DEFINE 8250 ACE BITS

807X ** 8250 UART CONTROL AND BIT DEFINITIONS.

808X

000.350 809X SC.ACE EQU 3500 SYSTEM CONSOLE PORT IF 8250 ACE

000.156 810X AC.DLY EQU 110 220 MIL. SEC. DELAY FOR 8250

811X

000.000 812X UR.RBR EQU 0 RECEIVER BUFFER REGISTER (READ ONLY)

000.000 814X UR.THR EQU 0 TRANSMITTER HOLDING REGISTER (WRITE ONLY)

MTR90-1 - H/Z-89 MONITOR
8251 USART BIT DEFINITIONS.

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815X	000.000	816X	UR.DLL	EQ	0	DIVISOR LATCH (LEAST SIGNIFICANT)
817X		818X	UR.DLM	EQ	1	DIVISOR LATCH (MOST SIGNIFICANT)
819X		820X	UR.IER	EQ	1	INTERRUPT ENABLE REGISTER
	000.001	821X	UC.EDA	EQ	00000001B	ENABLE RECEIVED DATA AVAILABLE INTERRUPT
	000.002	822X	UC.TRE	EQ	00000010B	ENABLE TRANSMIT HOLD REGISTER EMPTY INTERRUPT
	000.004	823X	UC.RSI	EQ	00000100B	ENABLE RECEIVE STATUS INTERRUPT
	000.010	824X	UC.MSI	EQ	00001000B	ENABLE MODEM STATUS INTERRUPT
		825X				
	000.002	826X	UR.IIR	EQ	2	INTERRUPT IDENTIFICATION REGISTER
	000.001	827X	UC.IIP	EQ	00000001B	INVERTED INTERRUPT PENDING (0 MEANS PENDING)
	000.006	828X	UC.IID	EQ	00000110B	INTERRUPT ID
		829X				
	000.003	830X	UR.LCR	EQ	3	LINE CONTROL REGISTER
	000.000	831X	UC.58H	EQ	00000000B	5 BIT WORDS
	000.001	832X	UC.68H	EQ	00000001B	6 BIT WORDS
	000.002	833X	UC.78H	EQ	00000010B	7 BIT WORDS
	000.003	834X	UC.88H	EQ	00000011B	8 BIT WORDS
	000.004	835X	UC.25B	EQ	00000100B	TWO STOP BITS SELECTED
	000.010	836X	UC.PEN	EQ	00001000B	PARITY COMPUTATION ENABLED
	000.020	837X	UC.EPS	EQ	00010000B	EVEN PARITY SELECT
	000.040	838X	UC.SKP	EQ	00100000B	STICK PARITY
	000.100	839X	UC.SB	EQ	01000000B	SET BREAK
	000.200	840X	UC.DLA	EQ	10000000B	DIVISOR LATCH ACCESS
		841X				
	000.004	842X	UR.MCR	EQ	4	MODEM CONTROL REGISTER
	000.001	843X	UC.DTR	EQ	00000001B	DATA TERMINAL READY
	000.002	844X	UC.RTS	EQ	00000010B	REQUEST TO SEND
	000.004	845X	UC.OU1	EQ	00000100B	OUT 1
	000.010	846X	UC.OU2	EQ	00001000B	OUT 2
	000.020	847X	UC.L00	EQ	00010000B	LOOP
		848X				
	000.005	849X	UR.LSR	EQ	5	LINE STATUS REGISTER
	000.001	850X	UC.DR	EQ	00000001B	DATA READY
	000.002	851X	UC.0R	EQ	00000010B	OVERRUN
	000.004	852X	UC.PE	EQ	00000100B	PARITY ERROR
	000.010	853X	UC.FE	EQ	00001000B	FRAMING ERROR
	000.020	854X	UC.BI	EQ	00010000B	BREAK INTERRUPT
	000.040	855X	UC.THE	EQ	00100000B	TRANSMITTER HOLDING REGISTER EMPTY
	000.100	856X	UC.TSE	EQ	01000000B	TRANSMITTER SHIFT REGISTER EMPTY
		857X				
	000.006	858X	UR.MSR	EQ	6	MODEM STATUS REGISTER
	000.001	859X	UC.DCS	EQ	00000001B	DELTA CLEAR TO SEND
	000.002	860X	UC.DDR	EQ	00000010B	DELTA DATA SET READY
	000.004	861X	UC.TER	EQ	00000100B	TRAILING EDGE OF RING
	000.010	862X	UC.0RL	EQ	00001000B	DELTA RECEIVE LINE SIGNAL DETECT
	000.020	863X	UC.CTS	EQ	00010000B	CLEAR TO SEND
	000.040	864X	UC.DSR	EQ	00100000B	DATA SET READY
	000.100	865X	UC.RI	EQ	01000000B	RING INDICATOR
	000.200	866X	UC.RLS	EQ	10000000B	RECEIVED LINE SIGNAL DETECT

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HARDWARE INTERRUPT VECTORS 10:41:12 17-FEB-82

869 *** INTERRUPT VECTORS.
870 *
871

873 ** LEVEL 0 - RESET
874 *
875 * THIS 'INTERRUPT' MAY NOT BE PROCESSED BY A USER PROGRAM.
876
877 ORG 00A

878
879 INIT0 JMP INIT0X DO H88 EXTENSION OF INITIALIZATION
880 INIT0.0 LXI H,PRGRAM+PRSL-1 (HL) = RAM DESTINATION FOR CODE
881 JMP INIT INITIALIZE
882
883 ERRPL INIT-1000A BYTE IN WORD 10A MUST BE 0
884

886 ** LEVEL 1 - CLOCK
887
888 INT1 EQU 100 INTERRUPT ENTRY POINT
889
890 ERNZ *-11Q INTO TAKES UP ONE BYTE
891
892 CALL SAVALL SAVE USER REGISTERS
893 MVI D,0
894 JMP CLOCK PROCESS CLOCK INTERRUPT
895 ERNPL CLOCK-1000A EXTRA BYTE MUST BE 0
377.201

897 ** LEVEL 2 - SINGLE STEP
898 *
899 * IF THIS INTERRUPT IS RECEIVED WHEN NOT IN MONITOR MODE,
900 * THEN IT IS ASSUMED TO BE GENERATED BY A USER PROGRAM
901 * (SINGLE STEPPING OR BREAKPOINTING). IN SUCH CASE, THE
902 * USER PROGRAM IS ENTERED THROUGH (UIVEC+3)
903
904 INT2 EQU 20A LEVEL 2 ENTRY
905
906 ERNZ *-21A INT1 TAKES EXTRA BYTE
907

908
909 CALL SAVALL SAVE REGISTERS
910 LDAX D (A) = (CTLFLG)
911 SET CTLFLG
912 JMP STPRN STEP RETURN

MTR90-1 - H/Z-89 MONITOR #09.02.01. Unix H8ASM V1.4.1 5-Jul-80 Page 21
 HARDWARE INTERRUPT VECTORS 10:41:14 17-FEB-82

913 *** I/O INTERRUPT VECTORS.
 914 *
 915 * INTERRUPTS 3 THROUGH 7 ARE AVAILABLE FOR GENERAL I/O USE.
 916 *

917 * THESE INTERRUPTS ARE NOT SUPPORTED BY MTR89, AND SHOULD
 918 * NEVER OCCUR UNLESS THE USER HAS SUPPLIED HANDLER ROUTINES
 919 * (THROUGH UIVEC)
 920

921 ORG 30A

922
 000.030 303 045 040 923 INT3 JMP UIVEC+6 JUMP TO USER ROUTINE

924
 000.033 102 061 064 925 DB 1020,610,640,620,1020 PART NUMBER 444-142

927
 000.040 928 ORG 40A

929
 000.040 303 050 040 930 INT4 JMP UIVEC+9 JUMP TO USER ROUTINE

931
 000.043 044 122 116 932 DB 440,1220,1160,1020,440 SUPPORT CODE

934
 000.050 935 ORG 50A

936
 000.050 303 053 040 937 INT5 JMP UIVEC+12 JUMP TO USER ROUTINE

938
 939 DLY - DELAY TIME INTERVAL.

940 **
 941 * ENTRY (A) = HILLISECOND DELAY COUNT/2
 942 * EXIT NONE
 943 * USES A,F
 944 *
 945

946 ERRNZ *-53A

947
 000.053 365 948 DLY PUSH PSH SAVE COUNT
 000.054 257 949 XRA A DONT SOUND HORN
 000.055 303 143 002 950 JMP HRNO PROCESS AS HORN

952
 000.060 953 ORG 60A

954
 000.060 303 056 040 955 INT6 JMP UIVEC+15 JUMP TO USER ROUTINE

956
 957

000.063 076 320 958 GO. MYI A,C8,SSI+C8,CLI+C8,SPK OFF MONITOR MODE LIGHT
 000.065 303 235 001 959 JMP SSI1 RETURN TO USER PROGRAM

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70A

ORG

962

81+3EAIN

JMP

964

MTR90-1 - H/Z-89 MONITOR
MASTER CLEAR PROCESSING

#09.02.01.

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```

967 **      INIT - INITIALIZE SYSTEM
968 *
969 *      INIT IS CALLED WHENEVER A HARDWARE MASTER-CLEAR IS INITIATED.
970 *
971 *      SETUP MTR88 CONTROL CELLS IN RAM.
972 *      DECODE HOW MUCH MEMORY EXISTS, SETUP STACKPOINTER, AND
973 *      ENTER THE MONITOR LOOP.
974 *
975 *      ENTRY FROM MASTER CLEAR
976 *      EXIT INTO MTR88 MAIN LOOP
977
978 ERRNZ *-73Q
979
980 INIT      COPY *PRSRDM* INTO RAM
981 MOV M,A   MOVE BYTE
982 DCX H     DECREMENT DESTINATION
983 INR E     INCREMENT SOURCE
984 JNZ INIT  IF NOT DONE
985
986 SINC      EQU 4000A SEARCH INCREMENT
987
988 MVI D,SINCR/256 (DE) = SEARCH INCREMENT
989 LXI H,START-SINCR (HL) = FIRST RAM - SEARCH INCREMENT
990
991 *      DETERMINE MEMORY LIMIT.
992
993 INIT1     MOV M,A   RESTORE VALUE READ
994 DAD D     INCREMENT TRIAL ADDRESS
995 MOV A,M   (A) = CURRENT MEMORY VALUE
996 DCR M     TRY TO CHANGE IT
997 CMP M
998 JNE INIT1 IF MEMORY CHANGED
999
1000 INIT2    DCX H
1001
1002 SPHL      SET STACKPOINTER = MEMORY LIMIT -1
1003
1004 PUSH H    SET *PC* VALUE ON STACK
1005 LXI H,ERROR
1006 PUSH H    SET *RETURN ADDRESS*

```

```

1009 **          SAVALL - SAVE ALL REGISTERS ON STACK.
1010 *
1011 *          SAVALL IS CALLED WHEN AN INTERRUPT IS ACCEPTED, IN ORDER TO
1012 *          SAVE THE CONTENTS OF THE REGISTERS ON THE STACK.
1013 *
1014 *          ENTRY CALLED DIRECTLY FROM INTERRUPT ROUTINE.
1015 *          ALL REGISTERS PUSHED ON STACK,
1016 *          IF NOT YET IN MONITOR MODE, REGPTR = ADDRESS OF REGISTERS
1017 *          ON STACK.
1018 *          (DE) = ADDRESS OF CTLFLG
1019 *
000.004          ERRMI 132A-*
000.132          ORG   132A
000.132 343      1022 SAVALL XTHL      SET H,L ON STACK TOP
000.133 325      1023          PUSH D
000.134 305      1024          PUSH B
000.135 365      1025          PUSH PSM
000.136 353      1026          XCHG      (D,E) = RETURN ADDRESS
000.137 041 012 000 1027          LXI    H,10
000.142 071      1028          DAD     SP
1029
1030 **          REPLACE THESE INSTRUCTIONS WITH A JUMP AROUND THE NMI VECTOR JUMP
1031 *
1032 *          PUSH H          SET ON STACK AS 'REGISTER'
1033 *          PUSH D          SET RETURN ADDRESS
1034 *          LXI D,CTLFLG
1035 *          LDAX D          (A) = CTLFLG
1036
000.143 303 105 004 1037          JMP     SAVALLX      GO TO SAVALL EXTENSION
1038
1039 **          ENTRY POINT FOR THE Z80 NMI
1040 *
1041
1042          ERRNZ *-66H      Z80 NMI ADDRESS
1043
000.146 303 116 004 1044 NMIENT JMP     NMI
1045
000.000          ERRNZ SAVALLR-151A DO NOT CHANGE ORGANIZATION
1046
000.151          SAVALLR EQU *          SAVALL EXTENSION RETURN ADDRESS
1047
000.151 057      1050          CMA
000.152 346 060 1051          ANI      CB.MTL+CB.SSI      SAVE REGISTER ADDR IF USER OR SINGLE-STEP
000.154 310      1052          RZ              RETURN IF WAS INTERRUPT OF MONITOR LOOP
000.155 041 002 000 1053          LXI    H,2
000.160 071      1054          DAD     SP          (H,L) = ADDRESS OF 'STACKPTR' ON STACK
000.161 042 035 040 1055          SHLD  REGPTR
000.164 311      1056          RET

```

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 INTERRUPT TIME SUBROUTINES 10:41:17 17-FEB-82

```

1058 **      CUI - CHECK FOR USER INTERRUPT PROCESSING.
1059 *
1060 *      CUI IS CALLED TO SEE IF THE USER HAS SPECIFIED PROCESSING
1061 *      FOR THE CLOCK INTERRUPT.
1062
000.000      ERRNZ *-165A
1063
1064
040.010      SET .MFLAG      REFERENCE TO MFLAG
000.165      LDAX B          (A) = .MFLAG
000.000      ERRNZ UO.CLK-1   CODE ASSUMED = 01
000.166      RRC
000.167      CC              IF SPECIFIED, TRANSFER TO USER
1070
1071 *      RETURN TO PROGRAM FROM INTERRUPT.
1072
000.000      ERRNZ *-172A
1073
1074
000.172      INTXIT POP PSH   REMOVE FAKE 'STACK REGISTER'
000.173      POP PSH
1076
000.174      POP B
1077
000.175      POP D
1078
000.176      POP H
1079
000.177      EI
000.200      RET
  
```

MTR90-1 - H/2-89 MONITOR #09.02.01.
 PROCESS CLOCK INTERRUPTS

 1084 *** CLOCK - PROCESS CLOCK INTERRUPT
 1085 *
 1086 * CLOCK IS ENTERED WHENEVER A MILLISECOND CLOCK INTERRUPT IS
 1087 * PROCESSED.
 1088 *
 1089 * TICCNT IS INCREMENTED EVERY INTERRUPT.
 1090

 1091 ERNZ *-201A
 1092

 000.201 052 033 040 1093 CLOCK LHL D TICCNT
 000.204 043 1094 INX H
 000.205 042 033 040 1095 SHLD TICCNT INCREMENT TICCOUNT
 1096

 000.210 072 011 040 1097 LDA CTLFLG CLEAR CLOCK INTERRUPT FLIP-FLOP
 000.213 323 360 1098 OUT OP.CTL
 1099 * EXIT CLOCK INTERRUPT.
 1100 *

 1101
 1102 LXI B,CTLFLG
 1103 LOAX B (A) = CTLFLG
 1104 ANI CB.MTL
 1105 JNZ INTXIT IF IN MONITOR MODE
 1106 DCX B
 1107 ERNZ CTLFLG-.MFLAG-1
 1108 LOAX B (A) = .MFLAG
 1109 ERNZ UO.HLT-2000 ASSUME HIGH-ORDER
 1110 RAL
 1111 JC CLK4 SKIP IT
 1112

 1113 * NOT IN MONITOR MODE. CHECK FOR HALT
 1114

 000.234 076 012 1115 MVI A,10 (A) = INDEX OF *P* REG
 000.236 315 052 003 1116 CALL LRA. LOCATE REGISTER ADDRESS
 000.241 136 1117 MOV E,M
 000.242 043 1118 INX H
 000.243 126 1119 MOV D,M (D,E) = PC CONTENTS
 000.244 033 1120 DCX D
 000.245 032 1121 LOAX D
 000.246 376 166 1122 CPI MI.HLT CHECK FOR HALT
 000.250 302 165 000 1123 JNZ CUI1
 000.253 076 007 1124 MVI A,A.BEL DING BELL
 000.255 315 302 003 1125 CALL WCC
 000.260 076 110 1126 MVI A,MH* MH* FOR HALT
 000.262 315 302 003 1127 CALL WCC
 000.265 303 322 000 1128 JMP ERROR
 1129

 1130 *** IF HALT, BE IN MONITOR MODE
 1131 JE ERROR
 1132 * NONE OF THE ABOVE, SO ALLOW USER PROCESSING OF CLOCK INTERRUPT
 1133

 000.270 303 165 000 1134 CLK4 EQU *
 000.270 303 165 000 1135 JMP CUI1 ALLOW USER PROCESSING OF CLOCK
 1136

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 MEMORY TEST 10:41:19 17-FEB-82

```

1138 **      THIS IS ONLY A PORTION OF THE DYNAMIC RAM TEST!!
1139 *
1140 *      WAIT BEFORE MAKING ANOTHER LOOP
1141
000.273 041 000 000 1142 DYNEM6 LXI H=0
000.276 053 1143 DYNEM7 DCX H
000.277 174 1144 MOV A,H
000.300 265 1145 ORA L
000.301 302 276 000 1146 JNZ DYNEM7 IF (B,C) NOT ZERO
1147
000.304 303 167 007 1148 JMP DYNEM4 TRY AGAIN BY INCREMENTING ONCE MORE
1149
1150 **      HAVE A FAILURE PRIOR TO REACHING END OF MEMORY!
1151 *
1152 DYNEM9 XCHG
000.307 353 1153 LXI H,MSG.ERR DISPLAY ERROR MESSAGE
000.310 041 336 014 1154
1155 *      RETURN ADDRESS
1156 DB MI.LDXA,MI.LDXB
000.313 335 041 1157 DW DY9.3
000.315 160 011 1158 JMP DYMSG
000.317 303 265 007

```

MTR90-1 - H/Z-89 MONITOR #09.02.01.
MTR - MAIN EXECUTIVE LOOP.

```

1161 *** ERROR - COMMAND ERROR.
1162 *
1163 * ERROR IS CALLED AS A 'BAIL-OUT' ROUTINE.
1164 *
1165 * IT RESETS THE OPERATIONAL MODE, AND RESTORES THE STACK POINTER.
1166 *
1167 * ENTRY NONE
1168 * TO MTR LOOP
1169 * CTLFLG SET
1170 * .MFLAG CLEARED
1171 * USES ALL
1172
1173 ERRNZ *-322A
1174
1175 ERROR EQU *
1176 LXI H,.MFLAG
1177 MOV A,M (A) = .MFLAG
1178 ANI 3770-U0.DDU-U0.NFR RE-ENABLE DISPLAYS
1179 MOV M,A REPLACE
1180 INX H
1181 MVI M,CB.SSI+CB.MTL+CB.CLI+CB.SPK RESTORE *CTLFLG*
1182 ERNZ CTLFLG-.MFLAG-1
1183 EI
1184 LHLD REGPTR
1185 SPHL RESTORE STACK POINTER TO EMPTY STATE
1186 CALL ALARM ALARM FOR 200 MS

```

```

1188 ** MTR - MONITOR LOOP.
1189 *
1190
1191 ERRNZ *-344A
1192 EQU *
1193 MTR
1194 EI
1195
1196 MTR1 EQU *
1197 LXI H,MTR1
1198 PUSH H SET 'MTR1' AS RETURN ADDRESS
1199 JMP CKAUTO CHECK AUTO BOOT, IF NOT CONTROL BACK TO NEXT
1200 MTR.15 CALL TYPM5G PRINT 'H:'
1201
1202 MTR.2 CALL RCC READ A CONSOLE CHARACTER
1203 ANI 01011111B MAKE SURE ITS UPPER CASE TO MATCH TABLE
1204 LXI H,MTR1 LOOK UP CHARACTER IN *MTR1*
1205 MVI B,MTR1AL (B) = LENGTH OF TABLE
1206
1207 MTR.3 CMP M SEE IF CHARACTER FROM CONSOLE = TABLE ENTRY
1208 INX H HL = ADDRESS
1209 JZ MTR.4 IF EQUAL
1210
1211 INX H
1212 INX H
1213 DCR B SEE IF PAST END OF TABLE

```