Heathkit® Manual

for the

MULTIPORT SERIAL I/O CARD

Model H8-4

OPERATION 595-2248

HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

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INTRODUCTION

The Heath Model H8-4 Multiport Serial I/O Card is a 4-channel asynchronous serial interface for use with the Heath H8 Computer System. Each channel is fully programmable (including baud rate) and has its own input and output ports. Any channel is functionally independent of the other three channels. All four channels interface with RS-232C, plus channel Ø has a 20 mA current loop option.

The modern, digital design assures excellent accuracy and reliability to give you many years of trouble-free operation.

SPECIFICATIONS

SERIAL INTERFACE

Channels	3 EIA RS-232C. 1 RS-232 or 20 mA current loop. Each channel provides serial data and primary RS-232C handshake.
Output Levels	RS-232C.
Input Levels	RS-232C compatible.
Channel 0 only	20 mA active or passive receiver and transmitter. 300 baud, max.

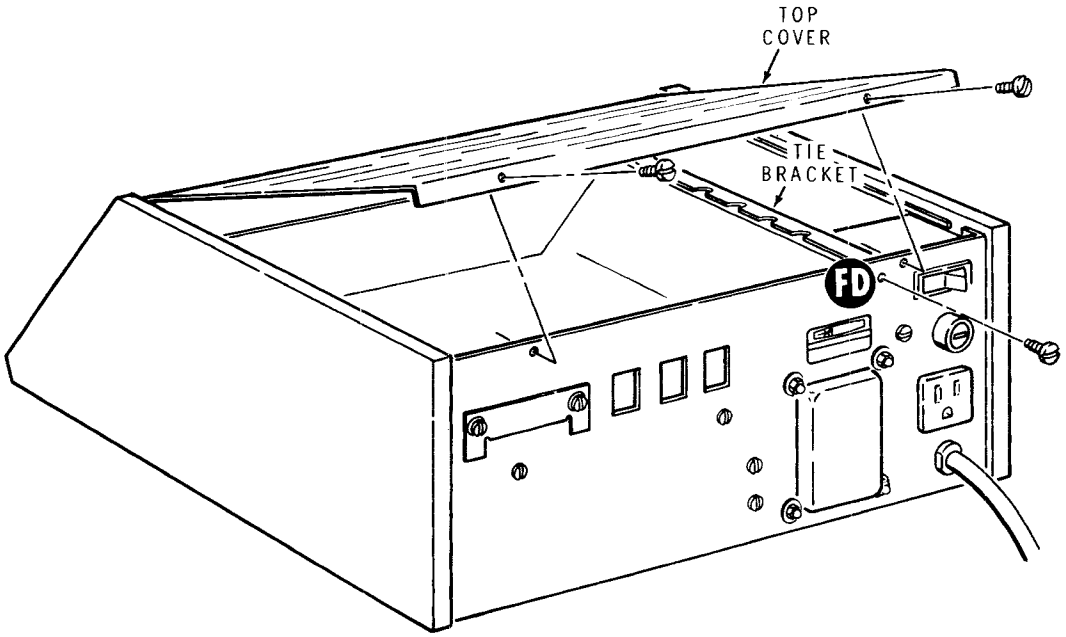
PROGRAMMABLE OPTIONS

Character Length	5, 6, 7, or 8 bits.
Parity	Even, odd, stick, or disabled.
Stop Bits	1, 1-1/2, or 2.
Baud Rates	Continuous, including all standard rates to 19,200 baud.

GENERAL

Computer Interface	For use with Heath H50 Bus.
Operating Temperature	0° — 40° Celsius.
Power Requirements	+8 volts DC at 580 mA. +18 volts DC at 75 mA. −18 volts DC at 60 mA.

INSTALLATION



PICTORIAL 1

Refer to Pictorial 1 for the following steps.

( ) Be sure your Computer is turned off.

( ) Remove the two rear panel screws holding the top cover and set the top cover aside if this has not already been done.

( ) Remove rear panel screw FD. Then loosen the other screws in the tie bracket, remove the bracket, and set it aside.

Refer to Pictorial 2 for the following steps.

NOTE: In the next step, you will install the Card into the Computer. Install the Card in one of the unused plugs near the rear of the Computer, but do not try to install it at P10. It will not fit.

( ) Plug the Multiport Serial I/O Card onto the selected plug in your Computer. NOTE: If you are also using the Serial I/O and Cassette Interface Card, plug in the Multiport Serial I/O Card one position in front of it.

( ) Refer to the "Heath System Configuration" section of this Manual and to the software that applies to this Card. Then set the programming jumpers and circuit board switches to their proper locations and positions.

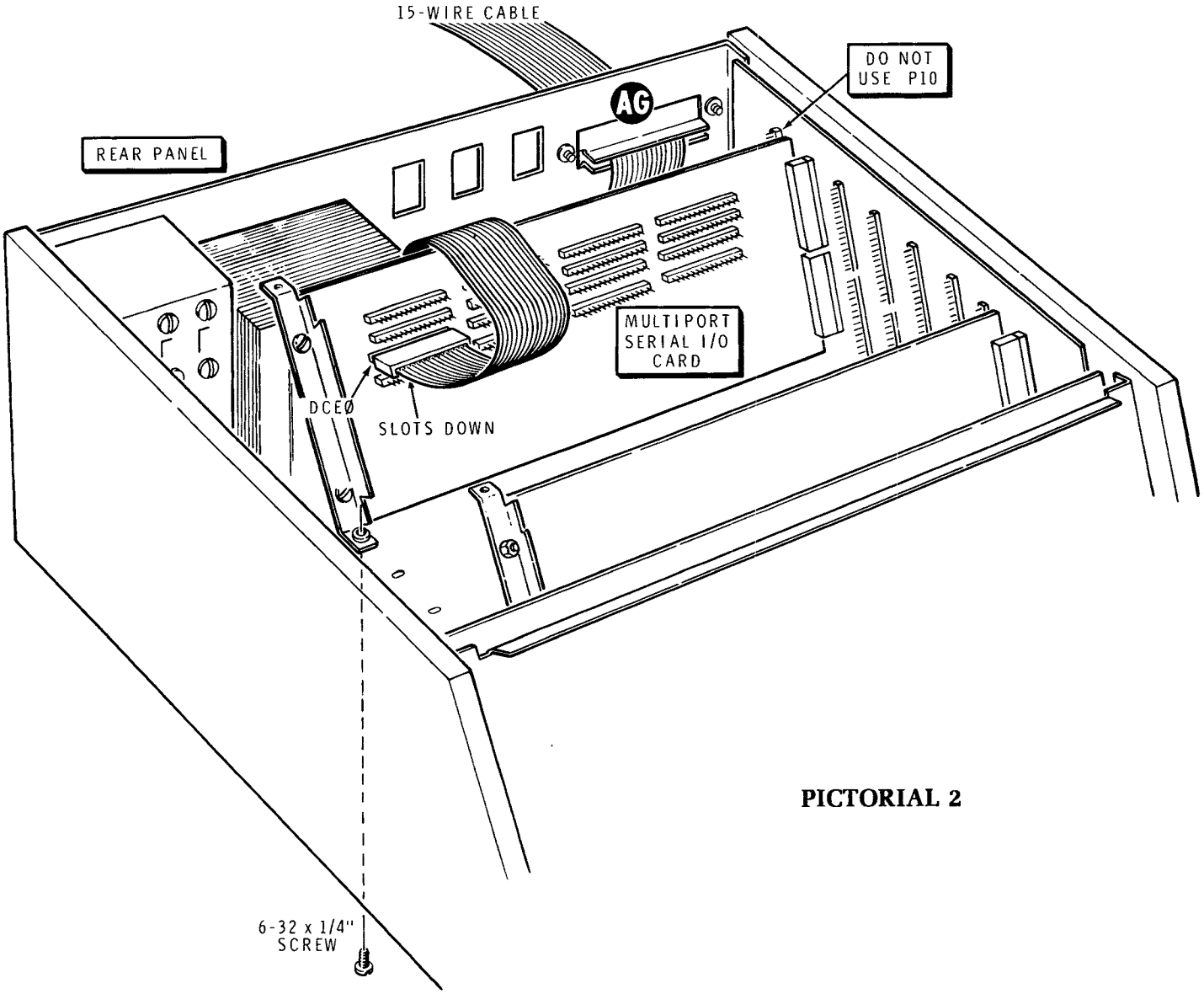
( ) Loosen the two screws of cable clamp AG, open the clamp, and route the flat connector of the 25-wire cable through the clamp.

( ) Plug the connector (slotted side as shown) onto the DCE pins of the channel you have chosen. (See "Operation" section.)

( ) In the same way, install any other accessory cables that you may have purchased.

( ) Close clamp AG until it is snug and retighten the screws.

( ) Install a 6-32 × 1/4" screw through the bottom of the computer chassis to hold the Card in place.



PICTORIAL 2

HEATH SYSTEM CONFIGURATION

To operate your Multiport Serial I/O Card, you must use the software written for this Card, correctly position the Card programming jumpers, and correctly connect the peripheral device (terminal, printer, etc.).

SOFTWARE REQUIREMENTS

CASSETTE OPERATION

Assembly Language (HASL-8), Text Editor (TED-8), and Console Debugger (BUG-8) are available on cassette (Heath Part #890-3, or higher). This cassette is supplied with the H8-18 software package. Benton Harbor Basic on this cassette **does not** operate with the H8-4.

Extended Benton Harbor Basic is avalable on cassette (Heath Part #890-4, or higher), and is supplied as part of HC8-14.

NOTE: The older 880-series cassettes will not work with this Card.

DISK OPERATION

Use only diskettes having Part#890-1-1 or higher, as supplied with the H8-17 software package. The older 890-1 diskettes will not work with this Card.

PROGRAMMING

Each type of peripheral device has a specific address assigned to it. These addresses are an integral part of the software, and the Multiport Card must be properly configured (with programming jumpers) before it will operate.

Refer to the following I/O address assignments and find the correct address for the type of peripheral that you want to connect. For example, the Heath software requires that a console terminal be assigned the address 350. Next, select which of the four channels you want to use (channel 0 through channel 3) and install programming jumpers on the address connectors (one of four sets of connectors along the top of the Card) to program the address. These jumpers will first and second digits of the address. The third digit is not selectable, but is understood to be zero. Pictorial 3 (Illustration Booklet, Page 1) shows a channel configured for address 350 on channel 3. Program jumpers are installed at 3 and 5.

TABLE OF I/O ADDRESS ASSIGNMENTS

DESCRIPTION	ADDRESS (OCTAL)
H8-4 Console terminal	350 (350-357)
H8-4 Line printer	340 (340-347)
H8-4 Alternate terminal 0	300 (300-307)
H8-4 Alternate terminal 1	310 (310-317)
H8-4 Alternate terminal 2	320 (320-327)
H8-4 Alternate terminal 3	330 (330-337)

NOTE: Any address may be assigned to any channel but two channels must not be assigned the same address.

Some peripheral devices require that you use interrupts. The software documentation will tell you which (if any) interrupts you need for each type of peripheral device. If a channel will not be using its interrupt function, store the jumper at the "OFF-INT" position of the address connectors. If a channel is not to be used at all, store the two address jumpers in the "OFF" positions. Pictorial 3 (Illustration Booklet, Page 1) shows examples. Channels 0 and 1 have interrupt 6 selected, channel 2 is off, and channel 3 has interrupt 3 selected. Remember, these are only example, — refer to your software manuals for your applications.

Check to be sure that the BOARD ENABLE jumper is placed in the "ON" position.

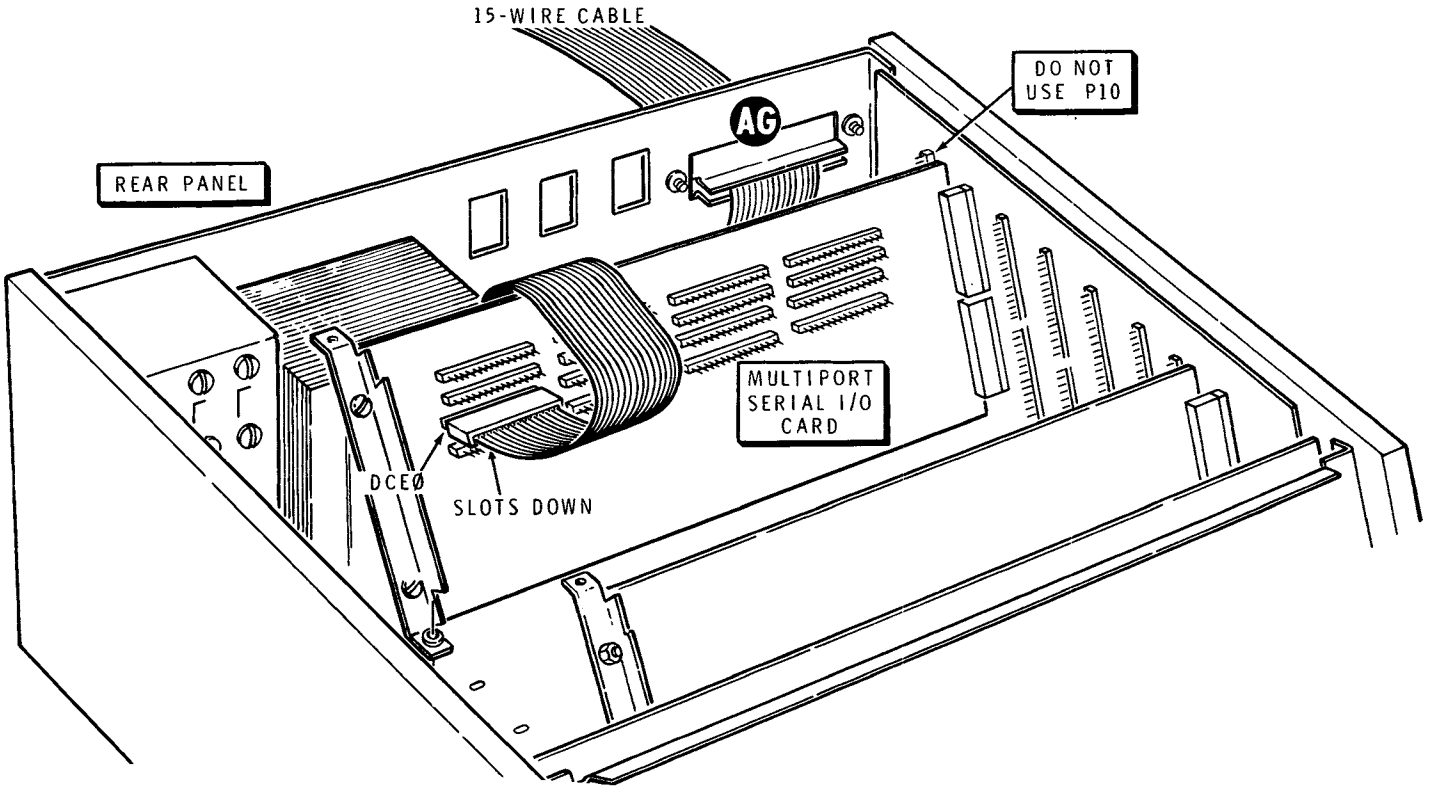
Be sure switch SW101 is in the RS-232 position.

PERIPHERAL INTERFACE

Peripheral devices connect to the I/O connectors of the Card with a 15-conductor flat cable that terminates in an EIA standard connector for RS-232 interface. One such cable is supplied; additional cable (WH8-41) are available from Heath Company. This cable mates with equipment using the standard RS-232 interface. To connect to an H9, a WH9-1 cable will be needed as shown in Pictorial 10 (Page 13).

The I/O connectors for each channel are located immediately below the address selection connectors. There are two connectors for each channel; the upper one is marked DCE (Data Communications Equipment) and the lower one is marked DTE (Data Terminal Equipment). Always use the DCE connector.

The cable connector that mates with the Multiport Card has slots along one of its surfaces. Always install the connector with these slots facing down. (See Pictorial 4.)



PICTORIAL 4

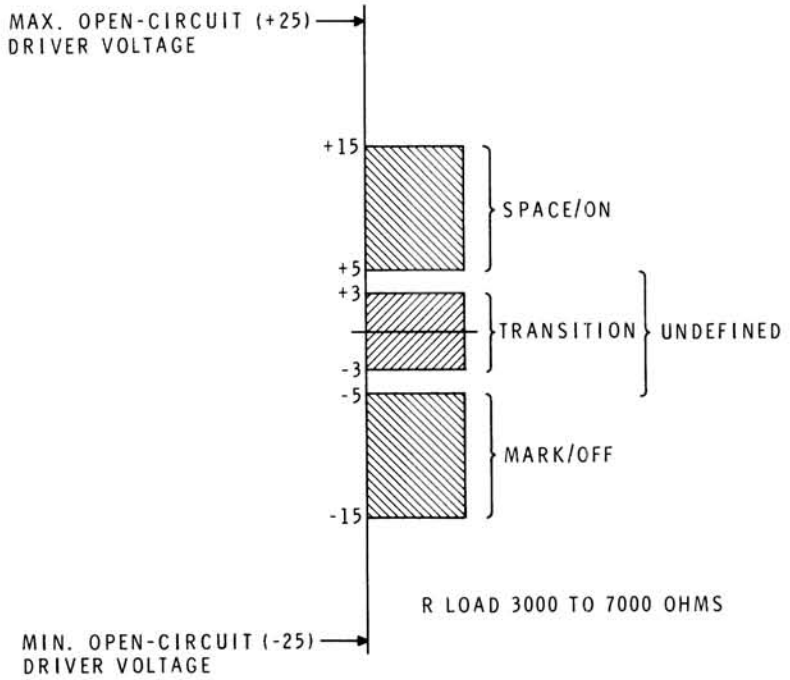
OPERATION

> The H8-4 Multiport Serial I/O Card requires new software that is specially designed to operate with it. This new software will work with either the H8-4 or H8-5 (Serial I/O and Cassette Interface Card). **Old** software **will not** work with the H8-4.

This section of the Manual is divided into four major sections:

- Interfacing
- Configuring with jumpers
- Programming
- Functional tests

INTERFACING



PICTORIAL 5

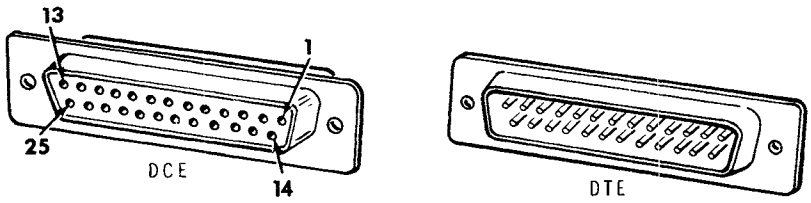
This card was designed to interface with peripherals using the RS-232C standards of the Electronic Industries Association. This standard defines an asynchronous serial interface, its voltages (see Pictorial 5), its impedances, and its physical connectors.

RS-232C places all equipment into one of two general categories:

DTE — Data Terminal Equipment.

DCE — Data Communication Equipment.

Computers and modems are two types of DCE; while terminals, printers, and most peripherals are DTE. Always connect a DTE to a DCE. Never connect two like types together.



PICTORIAL 6

Connectors (see Pictorial 6) are:

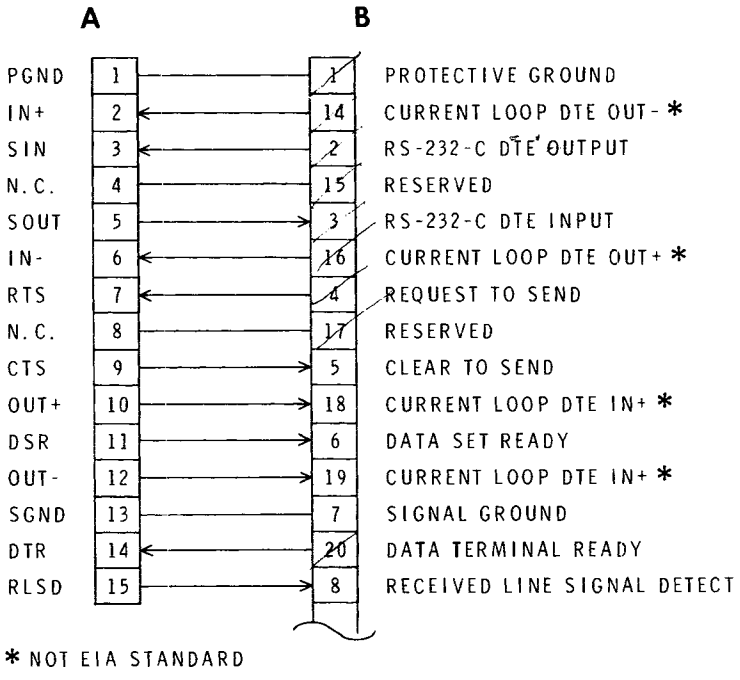
DCE — DB-25S (female pins)

DTE — DB-25P (male pins)

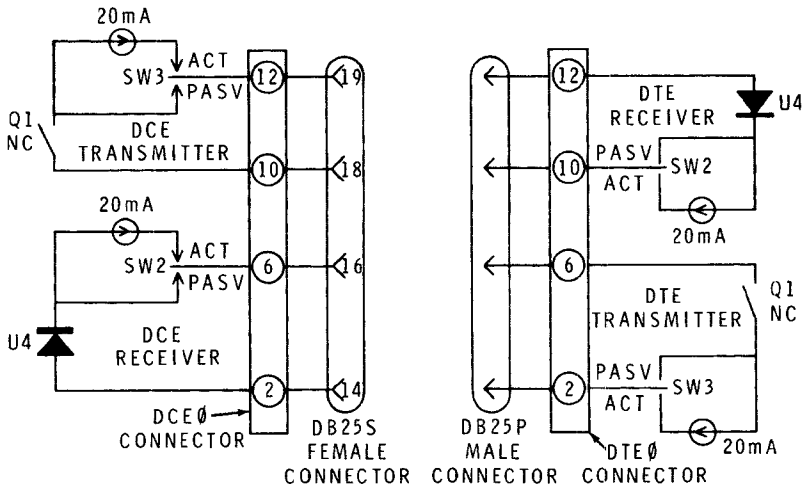
Pictorial 7 shows a DCE cable that will interface the Card with a DTE unit. End A is a 15-pin in-line connector that mates with a DCE plug on the card. End B is a 25-pin female "D" connector that mates with peripheral equipment.

20 mA CURRENT LOOP

You may configure channel Ø to operate in the 20 mA current mode. To do this, move circuit board switch SW1 from the RS-232 position to the 20 mA position. The current loop inputs and outputs will use four EIA unassigned pins of the H8-4 cable. See Pictorial 7.



PICTORIAL 7



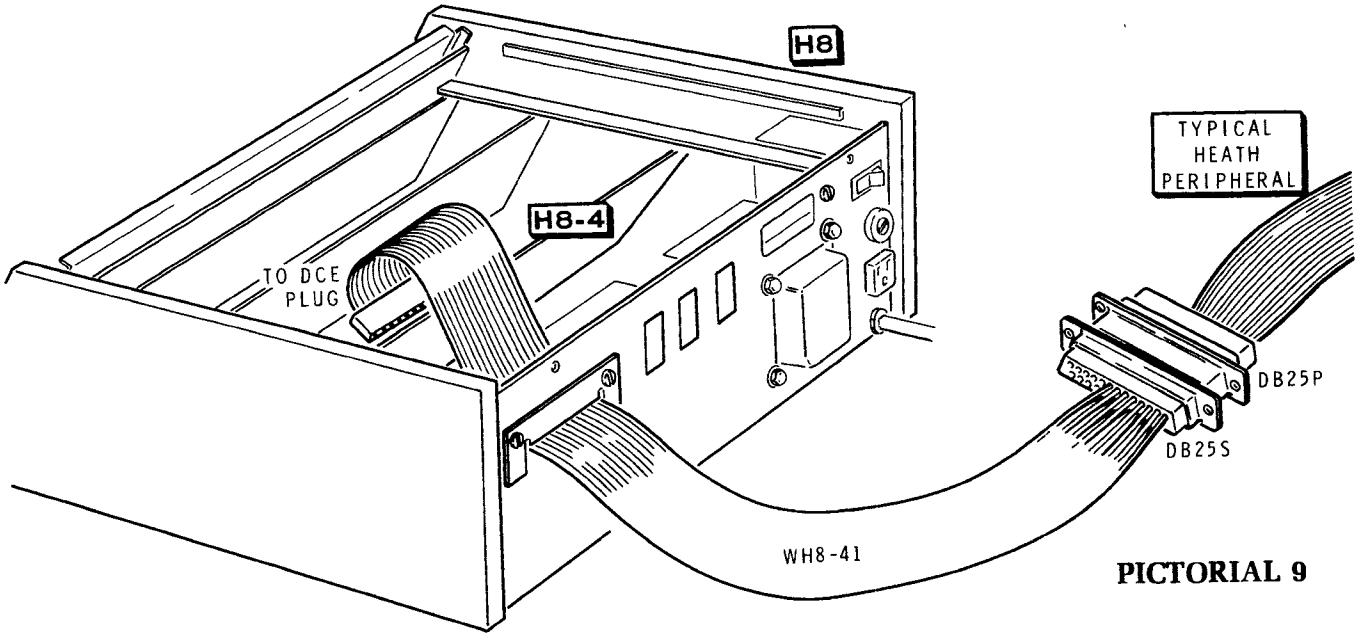
PICTORIAL 8

Pictorial 8 shows how a DCE transmitter can be connected to a DTE receiver, and a DCE receiver to a DTE transmitter. Each loop consists of a receiver, a transmitter, and a current source that are in series. A complete interface requires two independent loops, one loop for inputting data and one loop for outputting data.

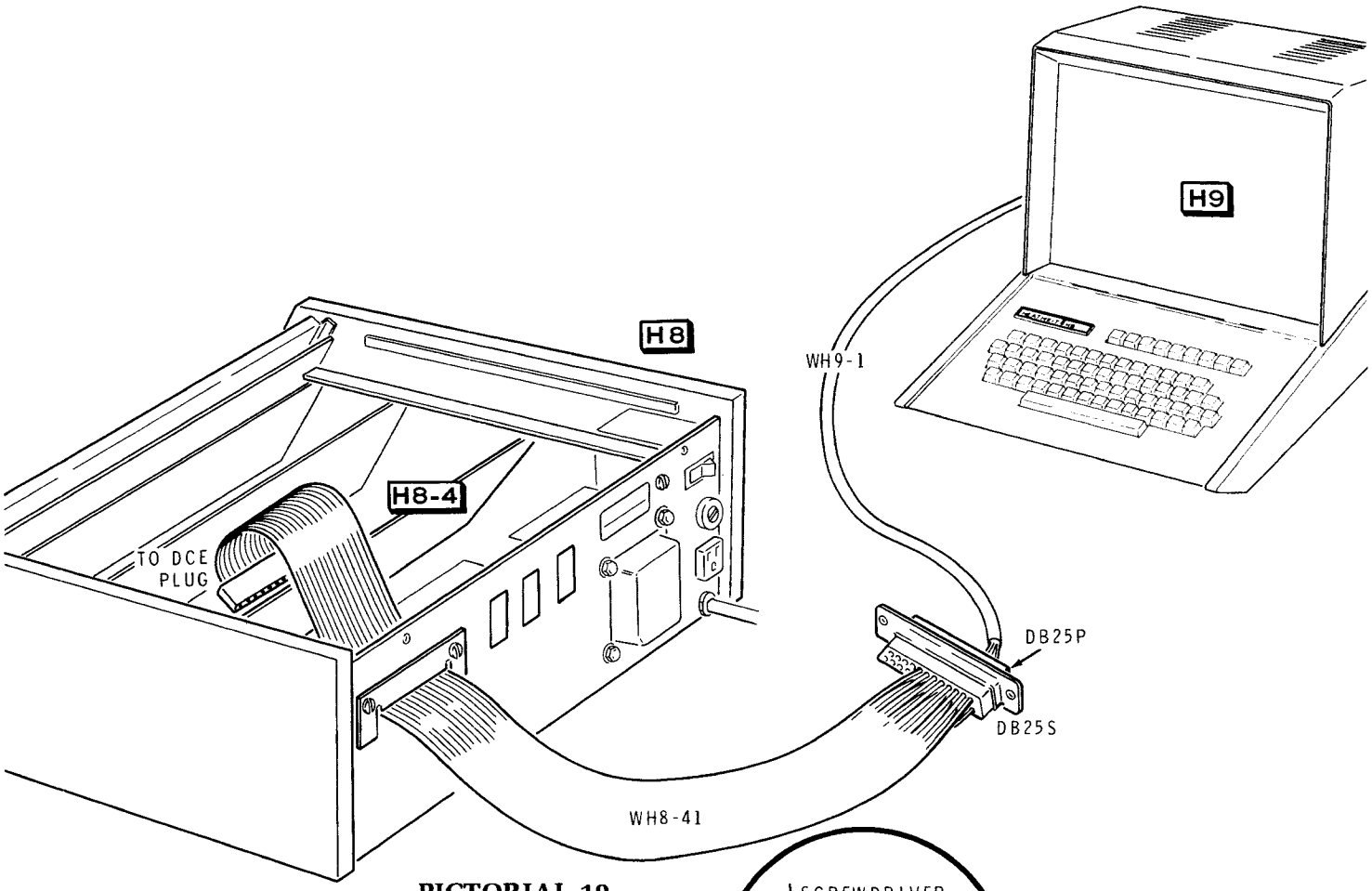
Each loop must have an active current source somewhere in the loop. This is usually nothing more than a voltage source and a series resistor. Only one current source is needed for each loop, and it is usually part of the transmitter or receiver. The part that contains the current source is **active** and the part without the source is **passive**. An external, independent source may be used and both the transmitter and receiver would be passive.

In the Multiport Serial I/O Card, switch SW2 selects either active or passive operation for the receiver, and switch SW3 selects either active or passive operation for the transmitter. The operation of the peripheral you connect will determine this selection.

A current loop interface is only suitable for use at low baud rates (300 maximum). For long cables, use lower baud rates.



PICTORIAL 9



PICTORIAL 10

HEATH PERIPHERALS

Most Heath DTE pheripherals can be connected to the Multiport Serial I/O Card with the H8-41 interface cable supplied with the card. See Pictorial 9.

H9 Terminal

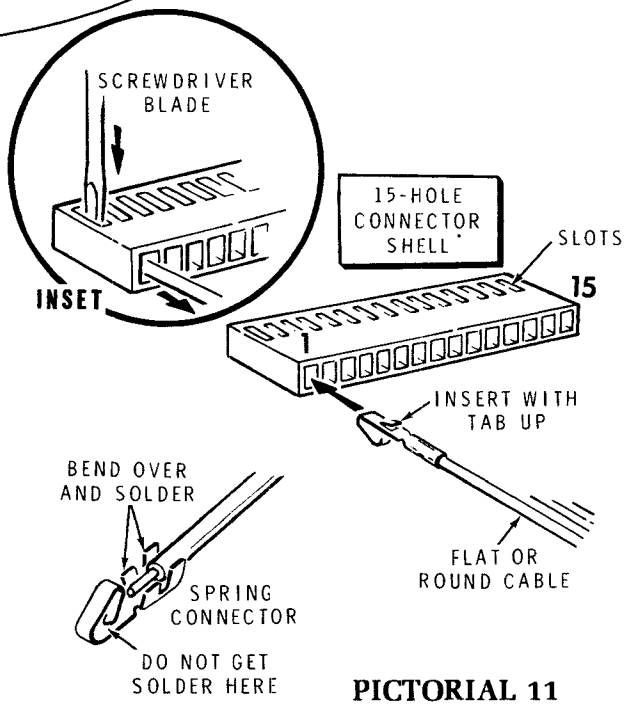
Refer to Pictorial 10 and connect the H9 to the H8-4 by using a WH9-1 adaptor cable as shown.

LA36 DEC Writer

The LA36 must be equipped with the EIA option. Then connect the D connector (DB25P) of the LA36 to the D connector (DB25S) of the H8-41 cable.

CUSTOM INTERFACING

Four 15-pin in-line connector shells (with pins) have been supplied to help you make custom I/O cables. See Pictorial 7 and the Schematic Diagram.



PICTORIAL 11

Pictorial 11 shows how to assemble the parts. The inset drawing shows how to remove a wire from a connector.

CONFIGURING WITH JUMPERS

Refer to Pictorial 12 (Illustration Booklet, Page 2) as you read the following material.

ADDRESS JUMPERS

The H8 system can address (communicate with) 256_{10} input/output devices by applying a unique binary code on 8 address lines ($2^8 = 256_{10}$). These codes, expressed in octal, represent the range 000 through 377.

Each channel of the H8-4 requires seven consecutive addresses. Thus, for example, if you choose a starting address of 350_8, the channel would require addresses 350 through 357. Therefore, it is only necessary to designate the highest and middle digits (DIG 1 and DIGIT 2) when you specify an address. When you use Heath software, the software documentation will specify the correct address.

The four channels (0, 1, 2, and 3) are identical, and any channel may operate at any address. **However, two channels may not be assigned the same address.** If you select your own addresses, do not use addresses used by other elements of your system.

The rows of address selection connectors are shown in Pictorial 12. Under DIG 1 (of each channel) are the numbers 0, 1, 2, and 3. These represent the most-significant digit of the address. This is the 3 in example address 350 as shown in Pictorial 12. Simply push the programming jumper down over the selected pair of pins as shown.

Under DIGIT 2 are eight pairs of pins (0 through 7). These represent the middle digit of the address (5 of example address 350).

The least significant digit is selected automatically. To disable a channel (which is good if it does not have an assigned address), place the DIG 1 and DIGIT 2 jumpers in the OFF positions. Channel 1 is shown in its OFF position in Pictorial 12.

INTERRUPT JUMPERS

The interrupt capability allows the serial interface to notify the computer that it requires service. This facility must be written into the software; it cannot be arbitrarily added by the user. Install the interrupt jumpers only when instructed to do so by the software documentation.

Pictorial 12 shows a group of interrupt pins for each channel. This allows each channel to be connected to interrupt 3, 4, 5, 6, or 7 independently of the other channels. More than one channel may be connected to the same interrupt when so instructed.

When the interrupt capability is not required, install the jumpers in the OFF-INT position of the center of the address selector.

Interrupt numbers 3 through 7 may appear as 30 through 70 in some documentation. This is the actual octal address that the CPU is sent to as the result of an interrupt.

Pictorial 12 shows channel $\not{0}$ set to interrupt 3, channel 1 to 6, channel 2 to 6, and channel 3 is OFF. Please note that these are only examples.

BOARD ENABLE

In the upper right-hand corner of the board is the BOARD ON/OFF (enable) jumper; it should normally be in the ON position. In the OFF position, the entire card, all parts and functions, will be disabled. This function may be useful for hardware or software debugging.

PROGRAMMING

When you use Heath software, you will not be concerned with programming the 8250 ACE (asynchronous communications element) in the H8-4. However, this section will be indispensable if you intend to assemble your own program code. (It is selected material from National Semiconductor and reprinted with their permission.)

INS8250 ACCESSIBLE REGISTERS

You (the system programmer) may access or control any of the INS8250 registers summarized in Table 1 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 Line Control Register

Specify the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, you may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1-1/2 Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This is the Parity Enable bit. When Bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This is the Divisor Latch Access bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud rate generator during a Read or Write operation. It must be set low (logic 0) to access the receiver buffer, the transmitter holding register, or the interrupt enable register.

Bit No.	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Table 1
Summary of INS8250 Accessible Registers.

8250 PROGRAMMABLE BAUD RATE GENERATOR

The 8250 contains a programmable baud rate generator that takes the 1.8432 MHz clock and divides it by any divisor from 1 to 2^{16} - 1. The output frequency of the baud generator is 16 × the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

Table 2 illustrates the standard baud rates and the contents of the LS (least significant) and MS (most significant) latches expressed in byte octal.

BAUD RATE	DIVISOR LATCH (LS)	(MS)
75	000	006
110	027	004
134.5	131	003
150	000	003
300	200	001
600	300	000
1200	140	000
2400	060	000
4800	030	000
9600	014	000
19200	006	000

Table 2
Baud Rates.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the line status register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the receiver buffer register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the receiver buffer register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the line status register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the line status register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the transmitter shift register is idle. It is reset to logic 0 upon a data transfer from the transmitter holding register to the transmitter shift register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the source of that interrupt are stored in the interrupt identification register (refer to table 3). The interrupt identification register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1. no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 3.

Bits 3 through 7: These five bits of the IIR are always logic 0.

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four interrupt sources of the INS8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt enable register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the interrupt identification register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the line status and MODEM status registers. The contents of the interrupt enable register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1. Bit 0 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1. Bit 1 is reset to logic 0 immediately upon reading the Interrupt Identification Register.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1. Bit 2 is reset to logic 0 upon completion of the associated interrupt service routine.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1. Bit 3 is reset to logic 0 upon completion of the associated interrupt service routine.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM control register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{\text{DTR}}$) output. When bit 0 is set to a logic 1, the $\overline{\text{DTR}}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{\text{DTR}}$ output is forced to a logic 1.

NOTE: The $\overline{\text{DTR}}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{\text{RTS}}$) output. Bit 1 affects the $\overline{\text{RTS}}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{\text{OUT 1}}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{\text{OUT 1}}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{\text{OUT 2}}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{\text{OUT 2}}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the transmitter shift register is "looped back" into the receiver shift register input; the four MODEM control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM control Interrupts are also operational but the interrupts sources are now the lower four bits of the MODEM control register instead of the four MODEM control inputs. The interrupts are still controlled by the interrupt enable register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the line status register and the lower four bits of the MODEM status register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM status register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM status register.

The contents of the MODEM status register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector, Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Table 3

Interrupt Control Functions.

FUNCTIONAL TESTS

These tests will thoroughly check the operation of your Multiport Serial I/O Card. Perform the tests if you think there is a problem on the Card or if you just want to be sure it is working properly before you start using it.

Refer to Pictorial 13 (Illustration Booklet, Page 3) and set the programming jumpers as follows:

Channel ø to øø.

Channel 1 to 11.

Channel 2 to 22.

Channel 3 to 33.

BOARD ON/OFF to ON.

All four INTERRUPTS to 5.

Set the three switches as follows:

RCV ACT/PASS to PASS.

XMT ACT/PASS to PASS.

20 mA/RS232 to RS232.

NOTES:

1. When RESET is called for in the ACTION column, simultaneously press the RST/ø and ø keys on the H8 front panel.

2. When ENTER is called for, first press the MEM key. (The H8 readout decimal points will light.) Then press the six keys in the order listed in the DIGITS ENTERED/EXPECTED DISPLAY column for the channel under test. After you enter the numbers, the decimal points will turn off.

3. The ACTION column will also call for the IN, OUT, +, and – keys to be pushed.

4. If the EXPECTED DISPLAY is correct, check YES and then proceed to the next test. If the display is not correct, check NO but continue on through the test. (This may help you in troubleshooting.) Then proceed to the "In Case of Difficulty" section on Page 36 of your Manual.

5. An asterisk (*) in these tests indicates a "don't care" condition where any number in the left six digits of the H8 readouts is acceptable.

6. The Data Readouts (three right-hand digits) are disregarded in these tests.

7. An X in a digit position denotes a "don't care" for that particular display.

8. Unless you have a difficulty, DO NOT turn off the H8 Power switch during the test.

There are six "Functional Tests." Tests one through five are divided into several sections (for channels ø-3). Perform all the steps for a channel before you proceed to the next channel, as shown by the arrows at the bottoms and tops of the columns.

If you make a keystroke error during a test sequence for a channel, you should reset and start the test over. It is not necessary to restart and go through all the tests.

Proceed to the "MULTIPORT SERIAL I/O CARD FUNCTIONAL TESTS" and perform the tests.

H8-4 MULTIPORT SERIAL I/O CARD FUNCTIONAL TESTS.

TEST # 1 - ACE Status after Reset:

The various registers in the 8250 ACE are placed in a known condition after a general reset. This test will verify each channel for proper status after reset.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)	CH2 (Y) (N)	CH3 (Y) (N)
RESET	RESET	RESET	RESET	RESET
ENTER	0.0.0. 0.0.0.	0.0.0. 1.1.0.	0.0.0. 2.2.0.	0.0.0. 3.3.0.
IN	X X X 0 0 0	X X X 1 1 0	X X X 2 2 0	X X X 3 3 0
+	X X X 0 0 1	X X X 1 1 1	X X X 2 2 1	X X X 3 3 1
IN	0 0 0 0 0 1 ( ) ( )	0 0 0 1 1 1 ( ) ( )	0 0 0 2 2 1 ( ) ( )	0 0 0 3 3 1 ( ) ( )
+	0 0 0 0 0 2	0 0 0 1 1 2	0 0 0 2 2 2	0 0 0 3 3 2
IN	0 0 1 0 0 2 ( ) ( )	0 0 1 1 1 2 ( ) ( )	0 0 1 2 2 2 ( ) ( )	0 0 1 3 3 2 ( ) ( )
+	0 0 1 0 0 3	0 0 1 1 1 3	0 0 1 2 2 3	0 0 1 3 3 3
IN	0 0 0 0 0 3 ( ) ( )	0 0 0 1 1 3 ( ) ( )	0 0 0 2 2 3 ( ) ( )	0 0 0 3 3 3 ( ) ( )
+	0 0 0 0 0 4	0 0 0 1 1 4	0 0 0 2 2 4	0 0 0 3 3 4
IN	0 0 0 0 0 4 ( ) ( )	0 0 0 1 1 4 ( ) ( )	0 0 0 2 2 4 ( ) ( )	0 0 0 3 3 4 ( ) ( )
+	0 0 0 0 0 5	0 0 0 1 1 5	0 0 0 2 2 5	0 0 0 3 3 5
IN	1 4 0 0 0 5 ( ) ( )	1 4 0 1 1 5 ( ) ( )	1 4 0 2 2 5 ( ) ( )	1 4 0 3 3 5 ( ) ( )
+	1 4 0 0 0 6	1 4 0 1 1 6	1 4 0 2 2 6	1 4 0 3 3 6
IN	0 0 0 0 0 6 ( ) ( )	0 0 0 1 1 6 ( ) ( )	0 0 0 2 2 6 ( ) ( )	0 0 0 3 3 6 ( ) ( )
+	0 0 0 0 0 7	0 0 0 1 1 7	0 0 0 2 2 7	0 0 0 3 3 7
IN	3 7 7 0 0 7 ( ) ( )	3 7 7 1 1 7 ( ) ( )	3 7 7 2 2 7 ( ) ( )	3 7 7 3 3 7 ( ) ( )

If all results were YES, go on to the next test. Otherwise, see the In Case of Difficulty Section.

TEST # 2 - Hardware Interrupt function:

The 8250 ACE generates an interrupt for any of several operations. This test checks the logic that places the interrupt on the H8 bus.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)	CH2 (Y) (N)	CH3 (Y) (N)
RESET	RESET	RESET	RESET	RESET
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.	0.2.0. 2.2.4.	0.2.0. 3.3.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4	0 2 0 2 2 4	0 2 0 3 3 4
IN	0 2 0 0 0 4 ( ) ( )	0 2 0 1 1 4 ( ) ( )	0 2 0 2 2 4 ( ) ( )	0 2 0 3 3 4 ( ) ( )
ENTER	0.1.7. 0.0.1.	0.1.7. 1.1.1.	0.1.7. 2.2.1.	0.1.7. 3.3.1.
OUT	BLANK with Tone sounding. ( ) ( )	BLANK with Tone sounding. ( ) ( )	BLANK with Tone sounding. ( ) ( )	BLANK with Tone sounding. ( ) ( )
RESET	RESET	RESET	RESET	RESET
MOVE	INT jumper CH0 to CH0 OFF INT	INT jumper CH1 to CH1 OFF INT	INT jumper CH2 to CH2 OFF INT	INT jumper CH3 to CH3 OFF INT

If there are any "NO" answers, refer to the In Case of Difficulty section.

TEST # 3 - Internal Control and Communication:

The internal loop back capability of the 8250 ACE will be used here to test the Control/Sense and Data paths inside the ACE.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)	CH2 (Y) (N)	CH3 (Y) (N)
RESET	RESET	RESET	RESET	RESET
ENTER	2.0.0. 0.0.3.	2.0.0. 1.1.3.	2.0.0. 2.2.3.	2.0.0. 3.3.3.
OUT	2 0 0 0 0 3	2 0 0 1 1 3	2 0 0 2 2 3	2 0 0 3 3 3
IN	2 0 0 0 0 3 (✓)( )	2 0 0 1 1 3 ( )( )	2 0 0 2 2 3 ( )( )	2 0 0 3 3 3 ( )( )
ENTER	0.0.0. 0.0.1.	0.0.0. 1.1.1.	0.0.0. 2.2.1.	0.0.0. 3.3.1.
OUT	0 0 0 0 0 1	0 0 0 1 1 1	0 0 0 2 2 1	0 0 0 3 3 1
IN	0 0 0 0 0 1 (✓)( )	0 0 0 1 1 1 ( )( )	0 0 0 2 2 1 ( )( )	0 0 0 3 3 1 ( )( )
ENTER	3.0.0. 0.0.0.	3.0.0. 1.1.0.	3.0.0. 2.2.0.	3.0.0. 3.3.0.
OUT	3 0 0 0 0 0	3 0 0 1 1 0	3 0 0 2 2 0	3 0 0 3 3 0
IN	3 0 0 0 0 0 (✓)( )	3 0 0 1 1 0 ( )( )	3 0 0 2 2 0 ( )( )	3 0 0 3 3 0 ( )( )
ENTER	0.0.3. 0.0.3.	0.0.3. 1.1.3.	0.0.3. 2.2.3.	0.0.3. 3.3.3.
OUT	0 0 3 0 0 3	0 0 3 1 1 3	0 0 3 2 2 3	0 0 3 3 3 3
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.	0.2.0. 2.2.4.	0.2.0. 3.3.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4	0 2 0 2 2 4	0 2 0 3 3 4
ENTER	0.1.7. 0.0.1.	0.1.7. 1.1.1.	0.1.7. 2.2.1.	0.1.7. 3.3.1.
OUT	0 1 7 0 0 1	0 1 7 1 1 1	0 1 7 2 2 1	0 1 7 3 3 1
ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.	0.0.0. 2.2.6.	0.0.0. 3.3.6.
IN	X X X 0 0 6	X X X 1 1 6	X X X 2 2 6	X X X 3 3 6
IN	0 0 0 0 0 6 (✓)( )	0 0 0 1 1 6 ( )( )	0 0 0 2 2 6 ( )( )	0 0 0 3 3 6 ( )( )
ENTER	0.3.7. 0.0.4.	0.3.7. 1.1.4.	0.3.7. 2.2.4.	0.3.7. 3.3.4.
OUT	0 3 7 0 0 4	0 3 7 1 1 4	0 3 7 2 2 4	0 3 7 3 3 4

TEST 3 (cont'd.)

ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.	0.0.0. 2.2.6.	0.0.0. 3.3.6.
IN	X X X 0 0 6	X X X 1 1 6	X X X 2 2 6	X X X 3 3 6
IN	3 6 0 0 0 6 ( )( )	3 6 0 1 1 6 ( )( )	3 6 0 2 2 6 ( )( )	3 6 0 3 3 6 ( )( )
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.	0.2.0. 2.2.4.	0.2.0. 3.3.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4	0 2 0 2 2 4	0 2 0 3 3 4
ENTER	1.7.7. 0.0.3.	1.7.7. 1.1.3.	1.7.7. 2.2.3.	1.7.7. 3.3.3.
OUT	1 7 7 0 0 3	1 7 7 1 1 3	1 7 7 2 2 3	1 7 7 3 3 3
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.	0.0.0. 2.2.2.	0.0.0. 3.3.2.
IN	0 0 6 0 0 2 ( )( )	0 0 6 1 1 2 ( )( )	0 0 6 2 2 2 ( )( )	0 0 6 3 3 2 ( )( )
ENTER	0.0.0. 0.0.5.	0.0.0. 1.1.5.	0.0.0. 2.2.5.	0.0.0. 3.3.5.
IN	1 7 1 0 0 5 ( )( )	1 7 1 1 1 5 ( )( )	1 7 1 2 2 5 ( )( )	1 7 1 3 3 5 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.	0.0.0. 2.2.2.	0.0.0. 3.3.2.
IN	0 0 4 0 0 2 ( )( )	0 0 4 1 1 2 ( )( )	0 0 4 2 2 2 ( )( )	0 0 4 3 3 2 ( )( )
ENTER	3.7.7. 0.0.0.	3.7.7. 1.1.0.	3.7.7. 2.2.0.	3.7.7. 3.3.0.
IN	0 0 0 0 0 0 ( )( )	0 0 0 1 1 0 ( )( )	0 0 0 2 2 0 ( )( )	0 0 0 3 3 0 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.	0.0.0. 2.2.2.	0.0.0. 3.3.2.
IN	0 0 2 0 0 2 ( )( )	0 0 2 1 1 2 ( )( )	0 0 2 2 2 2 ( )( )	0 0 2 3 3 2 ( )( )
IN	0 0 0 0 0 2 ( )( )	0 0 0 1 1 2 ( )( )	0 0 0 2 2 2 ( )( )	0 0 0 3 3 2 ( )( )
ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.	0.0.0. 2.2.6.	0.0.0. 3.3.6.
IN	0 1 7 0 0 6 ( )( )	0 1 7 1 1 6 ( )( )	0 1 7 2 2 6 ( )( )	0 1 7 3 3 6 ( )( )
ENTER	0.0.0. 0.0.2.	0.0.0. 1.1.2.	0.0.0. 2.2.2.	0.0.0. 3.3.2.
IN	0 0 1 0 0 2 ( )( )	0 0 1 1 1 2 ( )( )	0 0 1 2 2 2 ( )( )	0 0 1 3 3 2 ( )( )

TEST 3A - Internal Communication:

RESET	RESET	RESET	RESET	RESET
ENTER	2.0.0. 0.0.3.	2.0.0. 1.1.3.	2.0.0. 2.2.3.	2.0.0. 3.3.3.
OUT	2 0 0 0 0 3	2 0 0 1 1 3	2 0 0 2 2 3	2 0 0 3 3 3
ENTER	0.0.0. 0.0.1.	0.0.0. 1.1.1.	0.0.0. 2.2.1.	0.0.0. 3.3.1.
OUT	0 0 0 0 0 1	0 0 0 1 1 1	0 0 0 2 2 1	0 0 0 3 3 1
ENTER	3.0.0. 0.0.0.	3.0.0. 1.1.0.	3.0.0. 2.2.0.	3.0.0. 3.3.0.
OUT	3 0 0 0 0 0	3 0 0 1 1 0	3 0 0 2 2 0	3 0 0 3 3 0
ENTER	0.0.3. 0.0.3.	0.0.3. 1.1.3.	0.0.3. 2.2.3.	0.0.3. 3.3.3.
OUT	0 0 3 0 0 3	0 0 3 1 1 3	0 0 3 2 2 3	0 0 3 3 3 3
ENTER	0.2.0. 0.0.4.	0.2.0. 1.1.4.	0.2.0. 2.2.4.	0.2.0. 3.3.4.
OUT	0 2 0 0 0 4	0 2 0 1 1 4	0 2 0 2 2 4	0 2 0 3 3 4
ENTER	1.2.5. 0.0.0.	1.2.5. 1.1.0.	1.2.5. 2.2.0.	1.2.5. 3.3.0.
OUT	1 2 5 0 0 0	1 2 5 1 1 0	1 2 5 2 2 0	1 2 5 3 3 0
+	1 2 5 0 0 1	1 2 5 1 1 1	1 2 5 2 2 1	1 2 5 3 3 1
IN	0 0 0 0 0 1 (✓)( )	0 0 0 1 1 1 ( )( )	0 0 0 2 2 1 ( )( )	0 0 0 3 3 1 ( )( )
-	0 0 0 0 0 0	0 0 0 1 1 0	0 0 0 2 2 0	0 0 0 3 3 0
IN	1 2 5 0 0 0 (✓)( )	1 2 5 1 1 0 ( )( )	1 2 5 2 2 0 ( )( )	1 2 5 3 3 0 ( )( )
ENTER	2.5.2. 0.0.0.	2.5.2. 1.1.0.	2.5.2. 2.2.0.	2.5.2. 3.3.0.
OUT	2 5 2 0 0 0	2 5 2 1 1 0	2 5 2 2 2 0	2 5 2 3 3 0
+	2 5 2 0 0 1	2 5 2 1 1 1	2 5 2 2 2 1	2 5 2 3 3 1
IN	0 0 0 0 0 1 (✓)( )	0 0 0 1 1 1 ( )( )	0 0 0 2 2 1 ( )( )	0 0 0 3 3 1 ( )( )
-	0 0 0 0 0 0	0 0 0 1 1 0	0 0 0 2 2 0	0 0 0 3 3 0
IN	2 5 2 0 0 0 (✓)( )	2 5 2 1 1 0 ( )( )	2 5 2 2 2 0 ( )( )	2 5 2 3 3 0 ( )( )

If all replies are YES, proceed to "External Loop Tests."

TEST # 4 - External Loop Functions:

SET RS-232/20mA Switch to the RS-232 position.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 (Y) (N)	CH1 (Y) (N)	CH2 (Y) (N)	CH3 (Y) (N)
PLACE Test Cable (connector slots down) between:	DCE0 & DTE0	DCE1 & DTE1	DCE2 & DTE2	DCE3 & DTE3
RESET	RESET	RESET	RESET	RESET
ENTER	2.0.0. 0.0.3.	2.0.0. 1.1.3.	2.0.0. 2.2.3.	2.0.0. 3.3.3.
OUT	2 0 0 0 0 3	2 0 0 1 1 3	2 0 0 2 2 3	2 0 0 3 3 3
ENTER	0.0.0. 0.0.1.	0.0.0. 1.1.1.	0.0.0. 2.2.1.	0.0.0. 3.3.1.
OUT	0 0 0 0 0 1	0 0 0 1 1 1	0 0 0 2 2 1	0 0 0 3 3 1
ENTER	3.0.0. 0.0.0.	3.0.0. 1.1.0.	3.0.0. 2.2.0.	3.0.0. 3.3.0.
OUT	3 0 0 0 0 0	3 0 0 1 1 0	3 0 0 2 2 0	3 0 0 3 3 0
ENTER	0.0.3. 0.0.3.	0.0.3. 1.1.3.	0.0.3. 2.2.3.	0.0.3. 3.3.3.
OUT	0 0 3 0 0 3	0 0 3 1 1 3	0 0 3 2 2 3	0 0 3 3 3 3
ENTER	0.1.7. 0.0.4.	0.1.7. 1.1.4.	0.1.7. 2.2.4.	0.1.7. 3.3.4.
OUT	0 1 7 0 0 4	0 1 7 1 1 4	0 1 7 2 2 4	0 1 7 3 3 4
ENTER	0.0.0. 0.0.6.	0.0.0. 1.1.6.	0.0.0. 2.2.6.	0.0.0. 3.3.6.
IN	X X X 0 0 6	X X X 1 1 6	X X X 2 2 6	X X X 3 3 6
IN	3 6 0 0 0 6 ( )( )	3 6 0 1 1 6 ( )( )	3 6 0 2 2 6 ( )( )	3 6 0 3 3 6 ( )( )
ENTER	1.2.5. 0.0.0.	1.2.5. 1.1.0.	1.2.5. 2.2.0.	1.2.5. 3.3.0.
OUT	1 2 5 0 0 0	1 2 5 1 1 0	1 2 5 2 2 0	1 2 5 3 3 0
+	1 2 5 0 0 1	1 2 5 1 1 1	1 2 5 2 2 1	1 2 5 3 3 1
IN	X X X 0 0 1	X X X 1 1 1	X X X 2 2 1	X X X 3 3 1
-	X X X 0 0 0	X X X 1 1 0	X X X 2 2 0	X X X 3 3 0
IN	1 2 5 0 0 0 ( )( )	1 2 5 1 1 0 ( )( )	1 2 5 2 2 0 ( )( )	1 2 5 3 3 0 ( )( )

Proceed with Channel-to-Channel Communication tests if no failures were encountered.

TEST # 5 - Channel-to-Channel Communication:

ACTION	DIGITS ENTERED/EXPECTED DISPLAY CH0 & 3 (Y)(N)	CH0 & 2 (Y)(N)	CH0 & 1 (Y)(N)
CONNECT	DCE0 & DTE3	DCE0 & DTE2	DCE0 & DTE1
RESET	RESET	RESET	RESET
ENTER	2.0.0. 0.0.3	2.0.0. 0.0.3.	2.0.0. 0.0.3.
OUT	2 0 0 0 0 3	2 0 0 0 0 3	2 0 0 0 0 3
ENTER	0.0.0. 0.0.1	0.0.0. 0.0.1.	0.0.0. 0.0.1
OUT	0 0 0 0 0 1	0 0 0 0 0 1	0 0 0 0 0 1
ENTER	3.0.0. 0.0.0.	3.0.0. 0.0.0.	3.0.0. 0.0.0.
OUT	3 0 0 0 0 0	3 0 0 0 0 0	3 0 0 0 0 0
ENTER	0.0.3. 0.0.3.	0.0.3. 0.0.3.	0.0.3. 0.0.3.
OUT	0 0 3 0 0 3	0 0 3 0 0 3	0 0 3 0 0 3
ENTER	2.0.0. 3.3.3.	2.0.0. 2.2.3.	2.0.0. 1.1.3.
OUT	2 0 0 3 3 3	2 0 0 2 2 3	2 0 0 1 1 3
ENTER	0.0.0. 3.3.1.	0.0.0. 2.2.1.	0.0.0. 1.1.1.
OUT	0 0 0 3 3 1	0 0 0 2 2 1	0 0 0 1 1 1
ENTER	3.0.0. 3.3.0.	3.0.0. 2.2.0.	3.0.0. 1.1.0
OUT	3 0 0 3 3 0	3 0 0 2 2 0	3 0 0 1 1 0
ENTER	0.0.3. 3.3.3.	0.0.3. 2.2.3.	0.0.3. 1.1.3.
OUT	0 0 3 3 3 3	0 0 3 2 2 3	0 0 3 1 1 3
ENTER	1.2.5. 0.0.0.	2.5.2. 0.0.0.	1.2.5. 0.0.0.
OUT	1 2 5 0 0 0	2 5 2 0 0 0	1 2 5 0 0 0
ENTER	0.0.0. 3.3.0.	0.0.0. 2.2.0.	0.0.0. 1.1.0.
IN	1 2 5 3 3 0 ( )( )	2 5 2 2 2 0 ( )( )	1 2 5 1 1 0 ( )( )
ENTER	2.5.2. 3.3.0.	1.2.5. 2.2.0.	2.5.2. 1.1.0.
OUT	2 5 2 3 3 0	1 2 5 2 2 0	2 5 2 1 1 0
ENTER	0.0.0. 0.0.0.	0.0.0. 0.0.0.	0.0.0. 0.0.0.
IN	2 5 2 0 0 0 ( )( )	1 2 5 0 0 0 ( )( )	2 5 2 0 0 0 ( )( )

Do Channel 0 20mA Loop test if this exercise had all YES answers.

TEST # 6 - Channel 0 20mA Loop Communication.

ACTION	DIGITS ENTERED/EXPECTED DISPLAY (Y) (N)	SWITCHES
CONNECT DCE0 & DTE0		
SET		RS-232/20mA Switch to 20mA.
SET		RCV Switch to PASSive.
SET		XMT Switch to PASSive.
RESET	RESET	
ENTER	2.0.0. 0.0.3.	
OUT	2 0 0 0 0 3	
ENTER	0.0.0. 0.0.1.	
OUT	0 0 0 0 0 1	
ENTER	3.0.0. 0.0.0.	
OUT	3 0 0 0 0 0	
ENTER	0.0.3. 0.0.3.	
OUT	0 0 3 0 0 3	
ENTER	1.2.5. 0.0.0.	
OUT	1 2 5 0 0 0	
IN	X X X 0 0 0 ( )( )	(The X X X should not be 1 2 5)
SET		XMT Switch to ACTive.
ENTER	2.5.2. 0.0.0.	
OUT	2 5 2 0 0 0	
IN	2 5 2 0 0 0 ( )( )	
SET		RCV Switch to ACTive.
ENTER	2.5.2. 0.0.0.	
OUT	2 5 2 0 0 0	
IN	X X X 0 0 0 ( )( )	(The X X X should not be 2 5 2)
SET		XMT Switch to PASSive.
ENTER	1.2.5. 0.0.0.	
OUT	1 2 5 0 0 0	
IN	1 2 5 0 0 0 ( )( )	

This completes the functional testing of all four channels.

CIRCUIT DESCRIPTION

Refer to the Schematic Diagram (on fold-in) and Block Diagram (Illustration Booklet, Page 4) as you read the following information.

The four channels of the Multiport Serial I/O Card are electrically identical except that channel O also has a 20 mA current loop option. The heart of each channel is the ACE (asynchronous communications element). It controls the timing and other critical functions. Because they operate the same, only one ACE will be described later.

DATA BUFFER CONTROL LOGIC

The read and write data buffer signals originate in D latch U144. The read data buffers are enabled when $\overline{\text{RBEN}}$ goes low, and the write data buffers are enabled when WBEN goes high.

Read

If no channel has been selected, the RD line of each channel (CHxRD) is high, the SELR.G (select reset, gated) is low, and Pin 6 of U144 is held high (disabled). When one of the four ACE's is selected, the read line (CHxRD) goes low, SELR.G goes high, and at the next $\phi 2$ positive transition, the $\overline{Q}$ (Pin 6) will go low and enable the read buffer. After the CHxRD signal returns high, SELR.G resets the latch and turns off the read buffer.

Write

When none of the four ACE's has been selected, the CHxSEL signals will all be low and hold the Q output of U144B high, independent of all other inputs to U144. When any of the ACE's are addressed, the CS (chip select) line from that unit goes high. When any of the $\overline{\text{CHxSEL}}$ signals go low, the $\overline{\text{CHSEL.G}}$ line goes high and U144 may now be altered. If $\overline{\text{IOW.G}}$ goes low during chip select, the Q output (WBEN.F) will be set low and WBEN high to turn on the data write buffers. The D input of U144 will also be low for the duration of the IOW signal and the $\phi 2$ signal to the U144 clock input will not change the status of the latch. The first $\phi 2$ negative transition after the $\overline{\text{IOW.G}}$ goes high will reset the latch and turn off the data bus driver.

DATA BUFFERS

Bidirectional buffers U152 and U151 invert the inverted bus data lines (pins 10-17, D0-D7) and isolate the on-board data lines from the bus. These buffered data bits are connected directly to the eight data lines of the four ACE's (U101, U111, U121, and U131). When the read buffer enable ($\overline{\text{RBEN}}$) line is low, the data buffers feed data from the Card to the data bus. When the write buffer enable (WBEN) is high, signals from the data bus are coupled through the buffers and applied to the four ACE's.

INTERRUPT DRIVERS

Five lines of the H8 bus (35-39) are CPU interrupts. By asserting one of these lines, a peripheral device (such as this Card), can request service from the CPU. Each ACE may be programmed to generate interrupts. These interrupt signals (ICHϕ, 1, 2, and 3) from the ACE's are connected to four open-collector nand gates (U148) where they are inverted and connected to the interrupt patch area. Here the interrupt signal

from any channel can be connected to any interrupt (3, 4, 5, 6, or 7). When no interrupt is desired, the interrupt programming jumpers may be stored at the "INT-OFF" location in the address jumper area. During reset and board disable, the outputs of the interrupt drivers are held high which disables all interrupt requests.

CONTROL BUFFER

Integrated circuit U146 serves as an inverting buffer for the control functions; $\overline{\text{RESET}}$, IOR (input/output read), IOW (input/output write), and $\phi 2$ (inverted phase two clock). This IC is a three-state device that is used only to receive bus signals. When control pin 13 is at a logic high, the four outputs are active. When the BOARD ON-OFF jumper is moved to OFF, the control line is set low and the four outputs of U146 float independent of their inputs. Then the RESET.G (reset gated) goes high because of pullup resistor R142. Thus, in this OFF condition, a continual reset signal is on the Card. $\overline{\text{IOR}}$.G also goes high (because of R143) and disables the data drivers, and $\overline{\text{IOW}}$.G goes high (because of R144) and disables the data buffers (U152, U151).

ADDRESS CIRCUITS

Address Buffers

8-line bi-directional noninverting buffer U141 is used only as an input buffer. It never drives the address bus. The inverted address signals are present at pins 30 through 37 of the H8 bus. The three lowest order bits (Aϕ-A2) are inverted by U145 and feed the three address lines of the ACE's. Decoding inside the ACE's provides one-of-seven address decoding (only six are used).

Address Decoders

Address lines A3-A5 are connected to 1-of-10 decoder U143 that is being used as a 1-of-8 decoder (0-7). The high order input line is connected to the onboard reset line. During reset, the output is driven to a number greater than seven and no address is selected.

The two highest address lines (6 and 7) are decoded by U142 into their four states (0-3). U142 is inhibited by the reset line just like U143.

The 12 outputs of the address decoders (U142 and U143) are routed to the address selector connectors for channels 0-3.

Address Selection

The state of the eight address lines selects one of the 256 discrete I/O address. $2^8 = 256_{10}$ or $000_8 - 377_8$; where the left or highest digit is represented by A7 and A6; the middle digit by A5, A4, and A3; and the least or right digit by A2, A1, and Aϕ.

Since each channel requires seven continuous addresses, only the first (highest) and middle digits need be selected. Placing the programming jumpers in the ϕ, 1, 2, or 3 position selects the decoded high digit from U142. Similarly, placing a jumper at one of the locations 0-7 of the second digit selects one of the eight outputs from U143. Placing the jumpers at the DIG1 and DIG2 OFF positions will disable the channel because no decoded address will have been selected.

SERIAL DATA CHANNELS

The four channels are electrically identical (except channel ϕ also has a crystal oscillator and a 200 mA current loop option). Therefore, only channel ϕ will be described.

Crystal Oscillator

Crystal Y101, resistors R101 and R102, capacitors C104 and C105, and part of U101 make up a 1.8432 MHz crystal oscillator that serves as the clock for the baud rate generators of the ACE's. Without this clock, none of the ACE's will operate.

20mA Current Interface

Switch SW1 (20mA/RS232) inserts a 20mA transmitter and receiver between U103 and U104, and channel I/O connectors DCE and DTE.

Receiver: A positive current from pin 1 to pin 2 of U4 turns on the internal light-emitting diode which, in turn, turns on the photo transistor. When the transistor turns on, its collector voltage swings from plus 12 volts to minus 12 volts. This signal is converted by Switch SW1 to pin 1 of U104 where it appears as a standard EIA input.

When Switch SW2 is in the active (ACT) position, the H8 power supplies provide the current source. Then, by connecting DCE pins 6 and 2 together, current flows through the photo diode. With Switch SW2 in the passive (PASS) position, an external current source is required.

Transmitter: When Pin 8 of U103 (serial out) is positive, the light-emitting diode of U5 is turned on, which turns on the photo transistor. This reduces the base-emitter voltage of Q1 and turns it off. Current then stops flowing from pin 10 to pin 12 of the DCE connector. When the serial out signal swings negative, the light-emitting diode turns off, which turns off the photo transistor. This allows current source Q2 to turn on Q1 and allow current to flow in the loop. Switch SW3 sets the current transmitter in the active mode (H8 supplies the current) or the passive mode (external device supplies the current).

SERIAL I/O CHANNELS

The ACE has three address lines that are connected directly to the buffered address lines; AØR, A1R, and A2R (restored). This permits the selection of the internal status and control registers when the unit has been enabled by CSØ and CS1. This CHØSEL.G signal is generated by taking pins 11 and 12 of U102 low simultaneously through the two connector blocks at the channel address connectors. $\overline{\text{CHØHD}}$ (Channel Ø high digit) may be connected to 0, 1, 2, or 3 for the first digit of the address code and CHØMD (middle digit) may be connected to 0 through 7 for the middle digit of the address code. When the address bus carries the binary code that corresponds to the two selected digits, the CSØ and CS1 pins of the ACE will be active.

When the ACE is active, the CS Out (chip select out) will go high and indicate that U101 has been selected. This signal is inverted by U102 and the $\overline{\text{CHØSEL}}$.R signal is applied to the data buffer control logic.

The $\overline{\text{CHØSEL}}$.R also drives two other gates of U102. These gates are connected to pin 19 DOSTR (Data out strobe) and pin 22 DISTR (Data in strobe).

When the $\overline{\text{IOR}}$.G signal is present with the $\overline{\text{CHØSEL}}$.R signal, the DISTR input is high and U101 is in the read mode. At that time, DDIS (Driver disable, Pin 24) goes low to enable the READ DATA buffer. Now the data from the internal register that has been selected by the address code on pins 26, 27 and 28 will be present on pins 1 through 8 and the H8 bus through the Data Read Buffer.

When the $\overline{\text{IOW}}$.G signal is present with $\overline{\text{CHØSEL}}$.R, the DOSTR line is set high and U101 is in the write mode. The data on Pins 1 through 8 (from the H8 bus through the Data Write buffers) will be stored in the internal register selected by address pins 26, 27, and 28.

Four outputs form U101, S out (pin 11), $\overline{\text{RTS}}$ (pin 32), $\overline{\text{DTR}}$ (pin 33) and $\overline{\text{RLSD}}$ (pin 38) are buffered by U103. Here they are converted from TTL levels to RS-232 (approximately ± 10 volts) and routed to the two I/O connectors DTEØ (data terminal equipment, channel Ø) and DCEØ (data communications equipment, channel Ø).

Four inputs to U101, S in (pin 10), $\overline{\text{CTS}}$ (pin 36), $\overline{\text{DSR}}$ (pin 37) and RLSD (pin 38) came from U104 where the RS-232 input levels are converted to TTL for U101.

The only signals on the Card that are not TTL logic levels are those between the RS-232 transmitter and receiver chips (U103 and U104) and the DTE/DCE connectors.

NOTE: The following material is selected material from National Semiconductor and reprinted with their permission.

INS8250 FUNCTIONAL PIN DESCRIPTION

The function of all INS8250 input/output pins are described in the following paragraphs. (See the INS8250 Block Diagram, Illustration Booklet, Page 5). Some of these descriptions reference internal circuits. A low in these descriptions represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

Input Signals

Chip Select (CSØ, CS1, $\overline{\text{CS2}}$), Pins 12 - 14: When CSØ and CS1 are high and $\overline{\text{CS2}}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{\text{ADS}}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{\text{DISTR}}$), Pins 22 and 21: When DISTR is high or $\overline{\text{DISTR}}$ is low while the chip is selected, this allows the CPU to read status information or data from a selected register of the INS8250.

NOTE: Only an active DISTR or $\overline{\text{DISTR}}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{\text{DISTR}}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{\text{DOSTR}}$), Pins 19 and 18: When DOSTR is high or $\overline{\text{DOSTR}}$ is low while the chip is selected, this allows the CPU to write data or control words into a selected register of the INS8250.

NOTE: Only an active DOSTR or $\overline{\text{DOSTR}}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{\text{DOSTR}}$ input permanently high, if not used.

Address Strobe ($\overline{\text{ADS}}$), Pin 25: When low, it provides latching for the Register Select (A0, A1, A2) and Chip Select (CSØ, CS1, $\overline{\text{CS2}}$) signals.

NOTE: An active $\overline{\text{ADS}}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{\text{ADS}}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 - 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain INS8250 registers. The DLAB is reset low when the Master Reset (MR) input is active (low); the DLAB must be set high by the system software to access the baud generator divisor latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, it clears all the registers (except the receiver buffer, transmitter holding, and divisor latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{\text{OUT 1}}$, $\overline{\text{OUT 2}}$, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$) are affected by an active MR input. (Refer to Table 4.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{\text{CTS}}$), Pin 36: The $\overline{\text{CTS}}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM status register. Bit 0 (DCTS) of the MODEM status register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the CTS bit of the MODEM status register changes state, an interrupt is generated if enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, it indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM status register. Bit 1 (DDSR) of the MODEM status register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the DSR bit of the MODEM status register changes state, an interrupt is generated if enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, it indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM status register. Bit 3 (DRLSD) of the MODEM status register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM status register.

NOTE: Whenever the RLSD bit of the MODEM status register changes state, an interrupt is generated if enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, it indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM status register. Bit 2 (TERI) of the MODEM status register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM status register.

NOTE: Whenever the RI bit of the MODEM status register changes from a high to a low state, an interrupt is generated if enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

Output Signals

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, it informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM control register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, it informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM control register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT\ 1}$), Pin 34: A user-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\ 1}$) of the MODEM control register to a high level. The $\overline{OUT\ 1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT\ 2}$), Pin 31: A user-designated output that can be set to an active low by programming bit 3 (OUT 2) of the MODEM control register to a high level. The $\overline{OUT\ 2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, it indicates that the chip has been selected by active CS$\emptyset$, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7 - D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the baud generator divisor latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by typing this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt sources has an active high condition: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the

Marking (logic 1) state upon a Master Reset operation.

Input/Output Signals

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 data bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1 - 7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 Are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low
	MODEM Signal Inputs	Bits 4 - 7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into Either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT} \cdot \text{RCLK} \cdot \text{DISTR}}$ (AT Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High
D_7 - D_0 Data Bus Lines	In TRI-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	TRI-STATE DATA (ACE to CPU) DATA (CPU to ACE)

Table 4

Reset Control of Registers and Pinout Signals.

IN CASE OF DIFFICULTY

This section of the Manual is divided into two parts. The first part, titled "Troubleshooting and Repair Precautions," points out the care that you should use when you service the unit to prevent damaging components.

The second part, titled "Troubleshooting Charts" gives a test program and troubleshooting charts to help you find the difficulty.

If the "Troubleshooting Charts" section does not help you locate the problem, read the "Circuit Description" and refer to the Schematic Diagram (fold-in) to help you determine where the trouble is.

Refer to the "Circuit Board X-Ray View" (Illustration Booklet, Page 12) for the physical location of parts on the circuit board.

NOTE: In an extreme case where you are unable to resolve a difficulty, refer to the "Customer Serivce" information inside the rear cover of the Manual. Your warranty is also located inside the rear cover.

TROUBLESHOOTING AND REPAIR PRECAUTIONS

1. Make sure you do not short any adjacent terminals or foils when you make test or voltage measurements. If a probe or test lead slips, for example, and shorts together two adjacent connections, it is very likely to damage one or more of the transistors, diodes, or IC's.

2. Be especially careful when you test any circuit that contains an IC or transistor. Although these components have an almost unlimited life when used properly, they are much more vulnerable to damage from excess voltage and current than many other parts.

3. Do not remove any components while the unit is turned on.

4. Use a voltmeter with a high input impedance when you measure voltages.

5. Never apply +5 volts or ground potentials to the output of any IC.

6. When you make repairs, make sure you eliminate the cause as well as the effect of the trouble. If, for example, you find a damaged resistor, be sure you find out what damaged the resistor. If the cause is not eliminated, the replacement resistor may also become damaged when you put the unit back into operation.

7. In several areas of the circuit boards, the foil patterns are quite narrow. When you unsolder a part to check or replace it, avoid excessive heat while you remove the part. A suction-type desoldering tool makes part removal easier.

COMPONENTS

To remove faulty resistors or capacitors; first clip them from their leads, then heat the solder on the foil and allow each lead to fall out of its hole. Preshape the leads of the replacement part and insert them into the holes in the circuit board. Solder the leads to the foil and cut off the excess lead lengths.

You can remove transistors in the same manner as resistors and capacitors. Make sure you install the replacement transistor with its leads in the proper holes. Then solder the leads quickly to avoid heat damage. Cut off the excess lead lengths.

FOIL REPAIR

To repair a break in a circuit board foil, bridge solder across the break. Bridge large gaps in the foil with bare wire. Lay the wire across the gap and solder each end to the foil. Carefully trim off any excess bare wire.

TROUBLESHOOTING CHARTS

If you have not already done so, refer to Page 21 and complete the "Functional Tests." Then continue with the following.

NOTE: Most IC's on the circuit board have duplicates. If you find an IC that you think is bad, substitute it with an IC of the same type from another channel.

If you checked "NO" during "Functional Test" number:

1 — For any horizontal row of "NO's," proceed to the "Difficulty Test Program," below. There, you will enter the test program at START and go through the "Troubleshooting Charts."

For any "NO's" in only one channel, proceed to the "Difficulty Test Program," enter the test program, and then perform tests A and B for the faulty channel in the "Troubleshooting Charts" (Illustration Booklet, Pages 6 through 11).

2 — Any "NO" indicates a fault in U148 or the ACE (U101, U111, U121, or U131) of one channel.

3 — For any horizontal row of "NO's," proceed to the "Difficulty Test Program," below. There, you will enter the test program and go through the "Troubleshooting Charts."

For any "NO's" in only one channel, proceed to the "Difficulty Test Program," enter the test program, and then perform tests A and B for the faulty channel in the "Troubleshooting Charts" (Illustration Booklet, Pages 6 through 11).

3A — For any horizontal row of "NO's," proceed to the "Difficulty Test Program," below. There, you will enter the test program and go through a portion of the "Troubleshooting Charts" (Illustration Booklet, Page 6) starting at ★. For any "NO's" in only one channel, replace the ACE of that channel (U101, U111, U121, or U131).

4 — Any "NO" indicates bad U1X3 (U103, U113, U123, or U133) or U1X4 (U104, U114, U124, or U134).

5 — Any "NO" indicates that one of the two ACE's being tested is bad.

6 — Any "NO" indicates a problem in the 20 mA current loop. Test U4, U5, D1, D2, D3, Q1, and Q2.

DIFFICULTY TEST PROGRAM

Use a logic probe and check U146 pin 3 for a logic low.

Press the reset buttons. The logic level should momentarily go high. If it does not, replace U146.

Load and run the following test program.

— If Functional Test 1 or 3 produced any horizontal row of "NO's," go to "START" in the "Troubleshooting Chart" in the Illustration Booklet and locate and correct the problem.

— If the tests produced "NO's" for only one channel, only perform "Troubleshooting Chart" tests A and B for that channel.

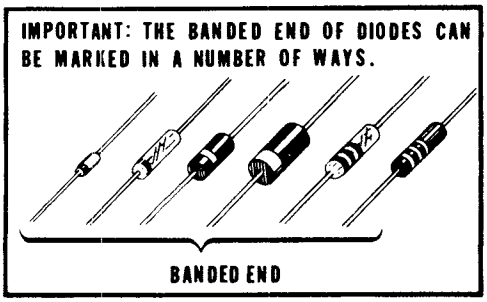
Test Program

ADDRESS		DATA		
040	100	363	START	DI
	101	041		LXI H, OPORT
	102	122		
	103	040		
	104	021		LXI D, IPORT
	105	124		
	106	040		
	107	006		MVI B, 125
040	110	125		
	111	066		MVI M, 357
	112	357		
	113	170	TEST	MOV A, B
	114	057		CMA
	115	107		MOV B, A
	116	064		INR M
	117	353		XCHG
040	120	064		INR M
	121	323		OUT OPORT
	122	000		
	123	333		IN IPORT
	124	000		
	125	303		JMP TEST
	126	113		
040	127	040		

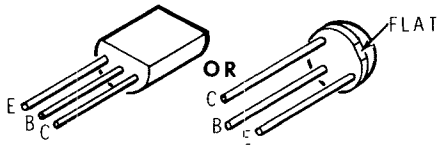
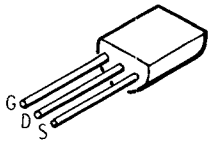
Set PC to 040 100 and press GO key.

SEMICONDUCTOR IDENTIFICATION CHARTS

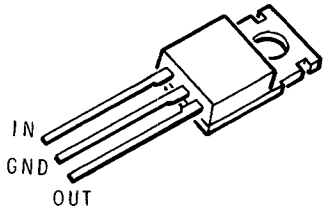
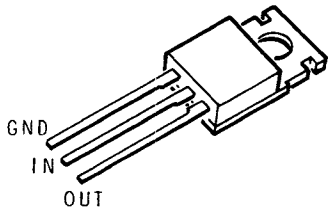
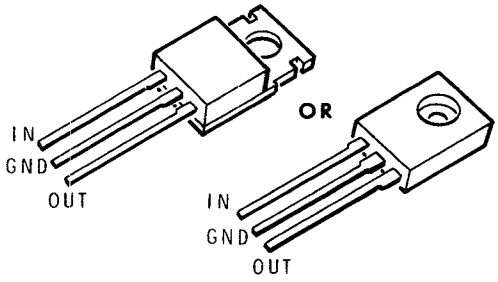
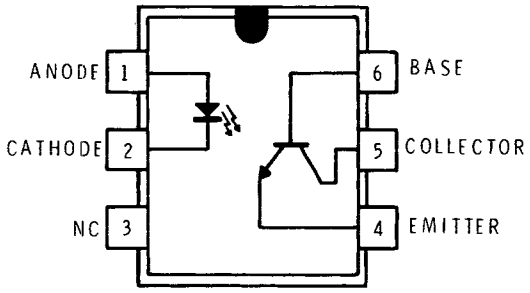
DIODES

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
D1, D3	57-65	1N4002	
D2	56-56	1N4149	

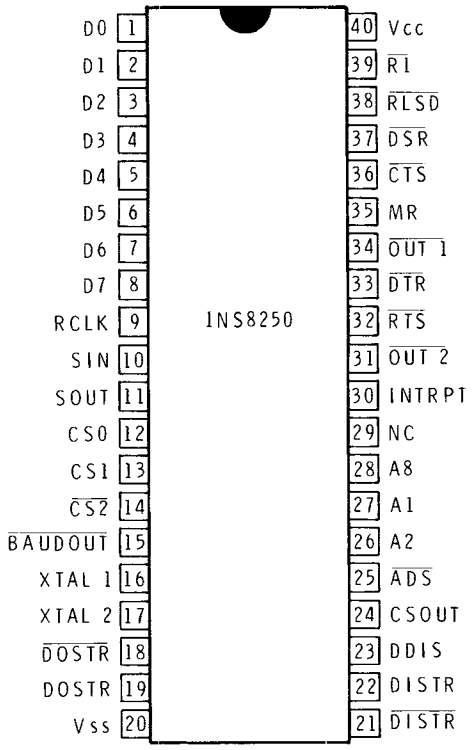
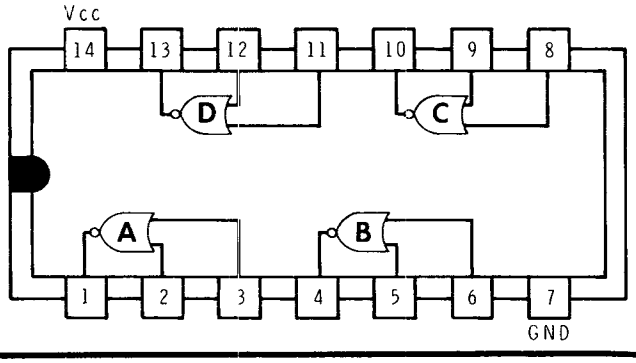
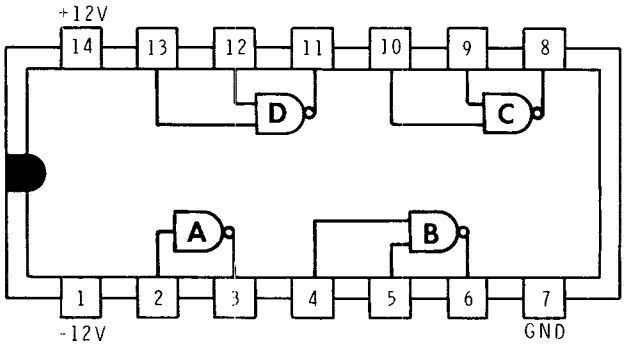
TRANSISTORS

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
Q1	417-865	MPS-A55	
Q2	417-897	N-Channel FET (selected)	

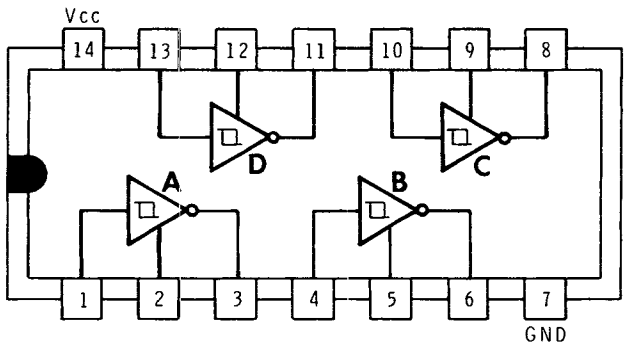
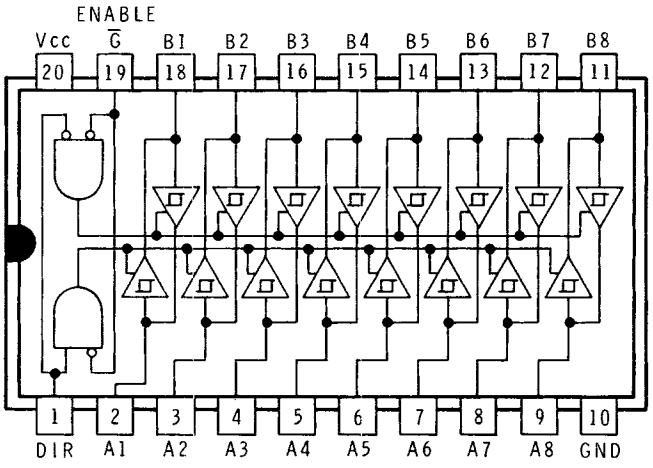
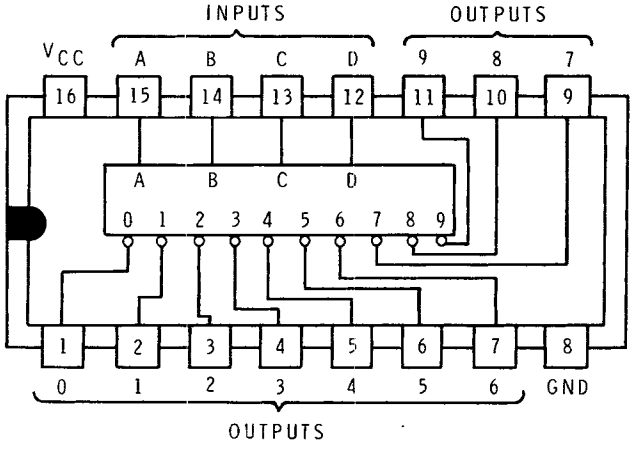
INTEGRATED CIRCUITS

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
U1	442-663	78M12	
U2	442-664	79M12	
U3	442-54	7805	
U4, U5	443-808	4N26	

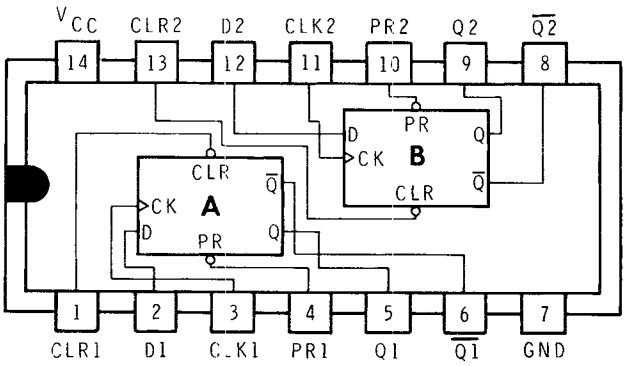
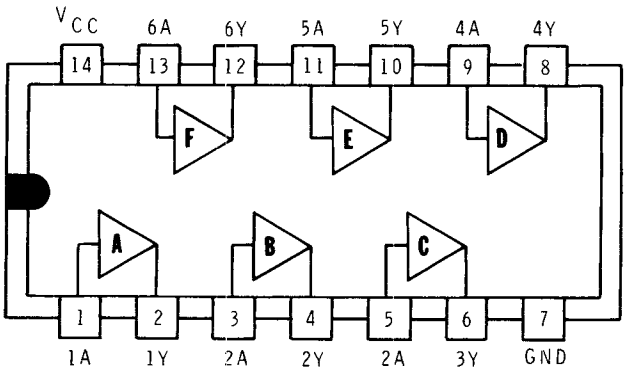
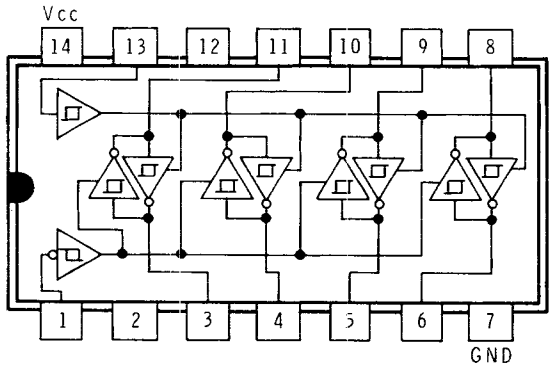
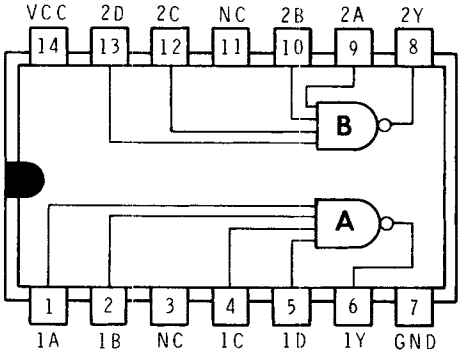
Integrated Circuits (cont'd.)

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
U101, U111, U121, U131	443-874	8250	
U102, U112, U122, U132	443-779	74LS02	
U103, U113, U123, U133	443-794	75188	

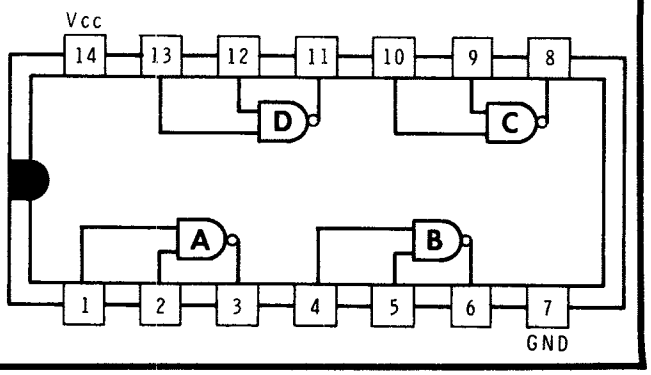
Integrated Circuits (cont'd.)

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
U104, U114, U124, U134	443-795	75189	
U141	443-885	74LS245	
U142, U143	443-807	74LS42	

Integrated Circuits (cont'd.)

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
U144	443-730	74LS74	
U145	443-755	74LS04	
U146, U151, U152	443-884	74LS242	
U147	443-798	74LS20	

Integrated Circuits (cont'd.)

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
U148	443-54	7403	

PARTS LIST

RESISTORS

(All resistors are 1/4-watt, 5% unless marked otherwise.)

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
R1	6-511	510 Ω, 1/2-watt
R2	6-511	510 Ω, 1/2-watt
R3	6-271-12	270 Ω
R4	6-104-12	100 kΩ
R5	6-222-12	2200 Ω
R6	6-222-12	2200 Ω
R7	6-104-12	100 kΩ
R8	6-511	510 Ω, 1/2-watt
R9	6-511	510 Ω, 1/2-watt
R101	6-152-12	1500 Ω
R102	6-105-12	1 MΩ
R141	6-102-12	1000 Ω
R142	6-102-12	1000 Ω
R143	6-102-12	1000 Ω
R144	6-102-12	1000 Ω

CAPACITORS

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
C1	25-221	2.2 μF tantalum
C2	25-221	2.2 μF tantalum
C3	25-221	2.2 μF tantalum
C4	25-221	2.2 μF tantalum
C5	25-221	2.2 μF tantalum
C6	25-221	2.2 μF tantalum
C101	21-95	.1 μF ceramic
C102	21-95	.1 μF ceramic
C103	21-143	.05 μF ceramic
C104	21-143	.05 μF ceramic
C105	21-147	47 pF ceramic
C106	21-147	47 pF ceramic
C111	21-95	.1 μF ceramic
C112	21-95	.1 μF ceramic
C113	21-143	.05 μF ceramic
C114	21-143	.05 μF ceramic
C121	21-95	.1 μF ceramic
C122	21-95	.1 μF ceramic
C123	21-143	.05 μF ceramic
C124	21-143	.05 μF ceramic
C131	21-95	.1 μF ceramic
C132	21-95	.1 μF ceramic
C133	21-143	.05 μF ceramic
C134	21-143	.05 μF ceramic
C141	21-95	.1 μF ceramic
C142	21-95	.1 μF ceramic
C143	21-95	.1 μF ceramic
C144	21-95	.1 μF ceramic
C145	21-95	.1 μF ceramic

DIODES — TRANSISTORS — IC'S

(See "Semiconductor Identification Chart.")

GENERAL

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
SW1	60-604	Switch
SW2	60-604	Switch
SW3	60-604	Switch
Y101	404-608	Crystal
	432-1038	Programming jumper