Instruction Manual

DG-FP8

Including:
DG-SS-1
DG-RD-1
FPM/80

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TABLE OF CONTENTS

The DG Electronic Developments Co. Model FP-8 is a hardware/firmware package designed for use with the DG-8Ø CPU board in the Heath H8 computer. The package consists of the following components:

FPM/8Ø Panel Monitor Firmware on a 2716 EPROM
DG SS-1 Front Panel Modification Board
DG RD-1 Disk Controller Modification Board

The FPM/8Ø Panel Monitor provides all features and functions of the Heath PAM-8 monitor as well as the following advanced features:

GENERAL FEATURES

Split octal or hexadecimal display & entry

Two keystroke display of memory contents pointed to by any register

Maintains all major PAM-8 entry points

User real time clock

Automatically sets PC register to disk system boot address on power-up

Provides software support for DG-ADP4 4 MHz disk system conversion

Provides software support for hardware assisted "single-step" operation

Z8Ø FEATURES

Display and alter all primary and alternate CPU registers

Display and alter index registers IX and IY

Provides for non-maskable interrupt entry

Support for Z8Ø 'Interrupt Mode 1'

Display and alter interrupt vector register

The DG-SS1 and DG-RD1 are modification boards used to support several of the features provided by the FPM/8Ø monitor. These boards "plug-in" in place of IC's on the appropriate H8 system boards and no alteration to the Heath circuit boards is required. (See the "System Installation" portion of this manual for more information on the SS1 and RD1 boards.)

The following operation information for the FPM/8Ø monitor is provided in a format and order similar to that used in the Heath PAM-8 Operation Manual. As mentioned previously, all standard PAM-8 features and functions are provided by FPM/8Ø and these are therefore not treated in detail in this manual. The user is referred to the appropriate section of the Heath PAM-8 manual for use of these functions. All unique FPM/8Ø features are discussed in the following pages.

NOTE: IT IS STRONGLY RECOMMENDED THAT THE USER REVIEW THE HEATH PAM-8 MANUAL BEFORE READING THIS MANUAL.

THEORY OF OPERATION

The DG-FP8 ROM contains two components:

1) Front panel monitor program--FPM/8Ø
2) System initialization program--SYSINIT.

The FPM/8Ø is normally furnished to operate from RAM in low memory, beginning at ØØØ ØØØ split octal. SYSINIT is provided in position independent code so that the FP8 ROM may be located at any location in the available memory space. A standard system would use the FP8 ROM and the Heath H17 disk ROM on the DG-8Ø CPU board with the CPU on-board memory address set to some location in high memory. (See the FP8 INSTALLATION INSTRUCTIONS portion of this manual for a discussion of ROM location considerations.) Upon system power-up or MASTER CLEAR, the following events will take place under SYSINIT:

1) SYSINIT transfers the contents of the Heath H17 disk ROM to low RAM beginning at Ø3Ø ØØØ split octal.
2) Using the Heath front panel 2ms clock, SYSINIT determines if the CPU is operating at the standard clock frequency of 2 MHz or the optional frequency of 4 MHz.
3) If the system is operating at 4 MHz, then timing-loop constants are patched in the H17 disk control area of memory.
4) The FPM/8Ø monitor and the remainder of SYSINIT are transferred to low RAM beginning at ØØØ ØØØ split octal.
5) The proper byte is written to I/O port Ø77 to turn off the CPU ROM and turn on all RAM of the DG-64D memory board (board ID Ø) if this board is being used. (Note that this byte will also turn off the CPU ROM if the DG-CMD1 ROM disable port is being used. This information will be ignored in systems not using the DG-64D or DG-CMD1 or in which port Ø77 is not being used.)
6) SYSINIT jumps to FPM/8Ø to begin the monitor setup.

SYSTEM OPERATION

CLOCK INTERRUPTS

As mentioned in the Heath PAM-8 manual, a 2ms hardware clock interrupt is provided by the H8 front panel. This clock interrupt is derived from the system clock frequency by dividing it by 4Ø96. Thus the time between hardware clock interrupts depends on the system clock frequency. Without modification, this hardware clock would occur once every 1ms if a 4.Ø96 MHz system clock were used. One purpose of the DG-SS1 modification board is to divide the system clock frequency by two when a 4 MHz system clock is used so the H8 front panel clock will always occur at approximately 2ms intervals.

USING RST & RTM

The RST and RTM commands of the FPM/8Ø are identical in function to those commands in PAM-8. The RST (MASTER CLEAR) is executed by simultaneously pressing the Ø and RST Ø (D) keys on the H8 front panel. The RTM function is a single key function in the FPM/8Ø to eliminate the occasional glitches present when using the double key PAM-8 RTM. The RTM function is executed by pressing the RTM (E) key.

FPM/8Ø DISPLAYS

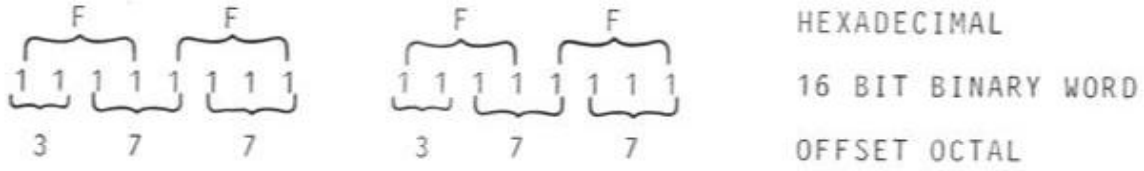
Upon power-up or MASTER CLEAR, the displays of the H8 computer using FPM/8Ø will be octal (offset octal for 16 bit quantities) as in PAM-8. However, the FPM/8Ø also provides an option of hexadecimal display. To enter the HEX display (and entry) mode, the user must press the FNCTN (C) key followed by the HEX (1) key. All displays

(register and memory) will then appear in hexadecimal until this two keystroke sequence is repeated.

Conversion from binary to octal to hexadecimal is as follows:

BINARY NUMBER	OCTAL NUMBER	HEX NUMBER
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	10	8
1001	11	9
1010	12	A
1011	13	B
1100	14	C
1101	15	D
1111	16	E
1111	17	F

Sixteen bit numbers may be converted to hexadecimal and offset octal as follows:



KEYPAD OPERATION UNDER FPM/80

The H8 keypad under FPM/80 operates as under PAM-8 with the following exceptions (see FIG. 1 for keypad layout)

1) The 'C' key on the front panel is used to enter the hex digit "C" when in hex entry mode: is used as a "FUNCTION" (FNCTN) key to select options requiring two keystrokes: or is used to cancel previous keypad entries as in PAM-8.

2) When in the hexadecimal alter mode, all keys represent digits (0 through F) until alteration is complete. (See altering memory locations section for clarification.)

3) Several keys control alternate modes of operation which will be described in the appropriate sections of this manual.

4) The 'repeat' rate of functions when holding keys down continuously has been doubled.

FIGURE 1

KEY TOPS FOR USE WITH FP8

DISPLAYING AND ALTERING MEMORY LOCATIONS

Upon power-up or MASTER CLEAR the Heath H8 will display the PC contents in octal display mode. Display and alteration of memory contents in the octal mode is identical to that using PAM-8. However, the FPM/8Ø monitor also allows display and alteration of memory contents in hexadecimal. This may be accomplished in the following manner:

1) To enter the hexadecimal display mode, press the FNCTN (C) key followed by the HEX (1) key.

2) To display a memory location, press the MEM (E) key followed by the four digit hexadecimal address desired. Note that when the MEM key is pressed while in the hexadecimal display mode, ALL keys are interpretted as legitimate character entries UNTIL four hex digits have been entered.

3) At this time, the four digit hexadecimal address will appear on the left-hand side of the display and the two-digit contents of this location will appear on the right-most two digits of the display:

REPRESENTATIVE EXAMPLE

4) To alter the contents of the displayed memory location, press the ALTER (D) key followed by the two hexadecimal digits representing the data byte desired. Note that when the ALTER key is pressed while in the hexadecimal display mode, ALL keys are interpretted as legitimate character entries until two hex digits have been entered. After two hex digits are entered the memory address increments by one and the ALTER mode is exited. Thus, the ALTER key MUST be pressed for EACH hex data byte entered into memory.

Stepping through memory using the + (A) key and the - (B) key is the same for the FPM/8Ø as the PAM-8 monitor except that if the hexadecimal display mode is being used, the ALTER key must be pressed to alter EACH location. Note that no efficiency of entry is lost using the hex entry mode since three keystrokes are required for data entry in either hex or octal entry mode.

DISPLAYING AND ALTERING REGISTERS

The FPM/8Ø monitor allows display and alteration of the 8Ø8Ø CPU registers as well as additional registers of the Z8Ø CPU. To specify a CPU register, press the REG (F) key followed by the register name given in the following table. The contents of the selected register will be displayed on the 6 left-most digits of the display when in the octal display mode (4 digits when in hexadecimal mode) and the register name will be displayed on the two left-most digits of the right hand group of displays: note that when in the memory display mode, hexadecimal data is displayed in the two right-most digits (left hand digit blank) and when in the register display mode, the register name is displayed in the two left-most digits (right hand digit blank) of the right hand group of H8 displays.

TABLE 1: REGISTER DISPLAY FORMAT

KEY	BYTE 1	BYTE 2	DISPLAYED NAME	COMMENTS
SP (1)	ØØØ THROUGH 377 ØØ FF	ØØØ THROUGH 377 ØØ FF	SP	STACK POINTER
AF (2)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	AF	AF REGISTER PAIR
BC (3)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	bC	BC REGISTER PAIR
DE (4)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	dE	DE REGISTER PAIR
HL (5)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	HL	HL REGISTER PAIR
PC (6)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	Pc	PROGRAM COUNTER
IX (7)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	IH	INDEX REGISTER X
IY (8)	ØØØ 377 ØØ FF	ØØØ 377 ØØ FF	IY	INDEX REGISTER Y

Note that the registers A, B, C, D, E, H, and L are eight bit registers and their values will lie in the range ØØØ through 377 octal or ØØ through FF hex. The program counter, stack pointer, index register X and index register Y are sixteen bit registers and will be displayed as 6 digit offset octal or four digit hexadecimal values.

Z80 ALTERNATE REGISTERS

The general purpose registers (A, B, C, D, E, H, L and the processor status word) have been duplicated in the Z8Ø microprocessor so that there is actually a 'primary' register set and an 'alternate' register set. Either of these register sets (but not both!) may be active at a given time. To select the contents of the alternate register set, press the FNCTN (C) key followed bye the REG' (3) key.

To return to the original contents of the primary registers, again press the FNCTN key followed by the REG' key. Each time this sequence is pressed, the contents of the two register sets are 'swapped' so that execution is always from the primary registers. When contents of the alternate register set are in use, the register name will be displayed with a prime symbol to the right,

PRIMARY AF becomes ALTERNATE AF'

AF AF'

NOTE: When the alternate register set is selected, prime symbols will be displayed with the PC, SP, IX, and IY registers although there are no alternates for these registers. These prime symbols serve only as a reminder that the alternate register set contents are in use.

ALTERING THE CONTENTS OF A SELECTED REGISTER

Altering register contents using the FPM/8Ø monitor is accomplished in the same manner as register alteration under PAM-8 when the octal display mode is used. Select the desired register, press the ALTER (D) key and punch in the six digits representing the desired register contents. When operating in hexadecimal display mode, press ALTER (D) followed by the four desired hexadecimal digits. Remember that when in the hexadecimal entry mode, all keys are interpretted as legitimate character entries until the current operation is completed. Therefore four digits must be entered (two bytes) before another monitor function is attempted. When the two bytes have been entered, the alter mode will be exited and the current register pair will continue to be displayed. Stepping

through the registers to view their contents may be accomplished using the + (A) key and the - (B) key as in PAM-8.

An additional register function available under FPM/8Ø is the XDSP function. When viewing the contents of a register pair (such as HL, BC, etc.) it is often desired to view the memory contents pointed to by the register pair contents interpretted as a memory address. This is accomplished by first viewing the desired register pair, then pressing the FNCTN (C) key followed by the XDSP (2) key. The display will then show the memory address represented by the register pair contents in the left-most six digits (4 digits when in the hex display mode) and the contents of that memory location in the right-most digits.

PROGRAM EXECUTION CONTROL

Execution of programs under FPM/8Ø is identical to that operation under PAM-8. To initiate program execution, place the address of the first instruction to be executed in the program counter and then press the GO (4) key. The computer will then execute instructions until a HALT instruction is executed (breakpointing) or the RTM function is selected from the front panel keypad. Of course, a MASTER CLEAR will also end program execution, however, NO register contents or flags will be preserved!

Single step operation is provided under the FPM/8Ø monitor by use of the DG-SS1 hardware modification board. With this modification, single step operation of the FPM/8Ø monitor is identical to that described for PAM-8. NOTE: The DG-SS1 hardware modification is absolutely necessary for single step operation of FPM/8Ø and

will not operate properly under PAM-8.

TAPE FACILITIES

Operation of the cassette tape facilities of FPM/8Ø is identical to that of PAM-8 with the exception of the RTM function which is not operational in the standard version of FPM/8Ø. A special version of FPM/8Ø (FPM/8ØT) is available from DG Electronic Developments Co. which provides the standard Heath RTM function. We refer the user to the Heath PAM-8 manual for a discussion of the tape facilities and their use.

I/O FACILITIES

Operation of the I/O facilities provided by FPM/8Ø is identical to that of PAM-8 when operating in the octal display mode. These same facilities are available also in the hexadecimal display mode using the hexadecimal entry instructions given in the memory section of this manual.

ADVANCED CONTROL

The following facilities of FPM/8Ø are exactly as described in the "ADVANCED CONTROL" section of the Heath PAM-8 manual:

16-BIT TICK COUNTER
USING THE KEYPAD
DISPLAY USAGE

USING INTERRUPTS

The Z8Ø microprocessor possesses several interrupt modes and features which are not available with the 8Ø8ØA microprocessor. A discussion of the three Z8Ø interrupt modes as well as the Z8Ø non-maskable interrupt (NMI) may be found in the DG Electronic Developments Co. DG-8Ø Z8Ø CPU instruction manual. The following

interrupt support is provided under the FPM/8Ø monitor:

Z8Ø INTERRUPT MODE Ø

This interrupt mode is identical to the single interrupt mode provided by the 8Ø8ØA microprocessor and is the mode in use upon power-up or MASTER CLEAR of the Z8Ø microprocessor. Operation of interrupts in this mode is identical to that described in the Heath PAM-8 manual. Refer to the FPM/8Ø source listing for specific information interrupt vectors.

Z8Ø INTERRUPT MODE 1:

Z8Ø Interrupt Mode 1 is discussed fully in the DG-8Ø Operation Manual. When operating the DG-8Ø in Interrupt Mode 1, all interrupts received are vectored via a CALL instruction through UIVEC+21. The contents of UIVEC+21 are initialized upon power-up or MASTER CLEAR to a RET instruction. If the user sets Interrupt Mode 1, he should first be sure to install the appropriate vector pointing to his handling routine.

Z8Ø INTERRUPT MODE 2:

No support is offered under FPM/8Ø for Z8Ø Interrupt Mode 2.

Z8Ø NON-MASKABLE INTERRUPT (NMI):

The Z8Ø CPU provides a non-maskable interrupt (i.e. this interrupt cannot be disabled through software) and this interrupt is supported under FPM/8Ø. All non-maskable interrupt requests are passed directly through UIVEC+24. Initially this vector is set to RETN (return from non-maskable interrupt) and should be set by the user when desired.

OTHER FPM/8Ø FACILITIES

H17 DISK SUPPORT:

The FPM/8Ø monitor provides software support for hardware assisted operation of the Heath H17 disk system at a CPU clock frequency of 4 MHz. The DG-ADP4 conversion module is required for 4 MHz operation.

H17 SYSTEM BOOT:

Upon power-up or MASTER CLEAR the program counter will be displayed on the H8 front panel and will contain the value ØØ4 365 split octal. If the GO (4) key is pressed at this time, disk system boot will begin. Disk system boot may be initiated when in the monitor mode by pressing the FNCTN (C) key followed by the BOOT (0) key. Thus it is not necessary to set the PC to any predetermined value to boot the system. These features are provided as a convenience to the user, however, the disk system may still be booted by entering the value Ø3Ø ØØØ split octal into the PC and then pressing the GO (4) key.

REAL-TIME CLOCK:

FPM/8Ø provides the user with a real time clock (SYSCLK), which is stored at a location pointed to by CLKPTR in the following format:

CLKPTR-4	HOURS	(0-23)
CLKPTR-3	MINUTES	(0-59)
CLKPTR-2	SECONDS	(0-59)
CLKPTR-1	MSEC/2	
CLKPTR+1	CLOCK TIMING CONSTANT	

NOTE: The values in the above table are actually displayed on the

H8 front panel in octal or hex, depending on the mode in use. Upon power-up or MASTER CLEAR, CLKPTR has the value Ø1Ø ØØ4 split octal. The clock timing constant represents the number of 2ms intervals (tics) that will be interpretted as 1 second. This constant may be altered by the user to compensate for disk system I/O or other interrupt disabling functions which might affect timing. The real time clock may also be moved by the user to other locations in memory by transferring CLKPTR-4 through CLKPRT+1 to the desired location and plugging the appropriate address into CLKPTR. (The user is referred to the FPM/8Ø source listing for further information.) Upon power-up or MASTER CLEAR, the clock is initialized to ØØ:ØØ:ØØ and may be set by the user by altering the appropriate memory locations. The clock also increments the date maintained in HDOS when midnight (24:ØØ:ØØ.ØØ) is reached, however, no provision is made for change of month.

MEMORY DISPLAY THROUGH INDIRECT ADDRESS:

Contents of a memory location pointed to by a 16 bit address made up of the contents of two consecutive memory locations may be viewed under FPM/8Ø by a simple two keystroke sequence. When viewing a memory location in the memory mode, press the FNCTN (C) key followed by the XDSP (2) key. This will cause the display to 'jump' to a memory address derived by using the displayed data byte as the low-order byte and the data byte contained in the next consecutive memory location as the high-order byte of a 16 bit memory address. For example, consider the following memory contents:

ADDRESS	DATA
Ø4Ø 1ØØ	3Ø3
1Ø1	11Ø
1Ø2	Ø4Ø
.	.
.	.
.	.
.	.
Ø4Ø 11Ø	ØØØ

The contents of location Ø4Ø 1ØØ represent a JUMP instruction for the 8Ø8ØA or Z8Ø CPU. If the user wished to view the contents of the location to be 'jumped to' using PAM-8, he would first increment the memory address to find the low-order byte 11Ø, increment the memory address once again to find the high-order byte Ø4Ø, then press MEM followed by the six digit address Ø4Ø 11Ø to find that the jump would be to the NOP instruction at that location. Under FPM/8Ø, the user would find the JUMP instruction at Ø4Ø 1ØØ, increment the memory address one location to the low-order byte, then press the FNCTN (C) key followed by the XDSP (2) key. The display will automatically 'jump' to the memory location Ø4Ø 11Ø and display the memory contents of that location.

INSTALLATION INSTRUCTIONS

Installation of the DG-FP8 firmware/hardware package is straightforward but does depend somewhat on the desired system configuration. The FP8 was designed primarily for use with the H8 incorporating the H17 disk system, however, the monitor (FPM/8Ø) will operate beautifully with the Heath cassette tape system as well. If you are not using the H17 disk system, then you should ignore the steps below marked with an asterisk (*). Always double check each step when performed and reread the instructions when in doubt about a specific step. Note that in some of the following steps you will remove and/or replace IC's. Proper care should be taken to avoid damage to these devices.

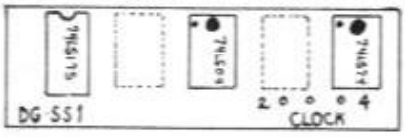
1) Turn off the H8 computer system completely and unplug the line cord.

2) Remove the computer top cover and tie bracket as well as the gray front cover. This front cover is held in place by two screws at the bottom and two screws just inside the computer at the top.

3) Examine the lower left hand corner of the Heath front panel circuit board and locate the following two IC's:

IC #	TYPE	HEATH PART #
1Ø8	7474	443-6
1Ø9	74LSØ4	443-755

4) Remove the above IC's from the front panel circuit board and install them in the DG-SS1 circuit board as shown in the figure below:



Note that pin 1 (the notched end) of each IC should be toward the top of the board.

5) Examine the CLOCK jumper on the DG-SS1 circuit board to determine if it is set to the clock frequincy you intend to use (either 2 or 4 MHz).

The jumper should connect from the center hole to the hole labelled with your desired clock frequency. Alter this jumper if necessary.

6) Plug the DG-SS1 circuit board into the IC sockets labelled IC 1Ø8 and IC 1Ø9 on the front panel circuit board. The board should plug in so that the writing on it is "right-side-up" as viewed from the front of the computer. Be very careful to line up the pins of the board plugs with the sockets on the front panel. DO NOT FORCE THE BOARD! It should fit snugly but not be difficult to plug in.

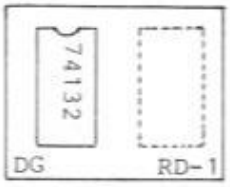
7) Examine the back side of the gray front cover of the computer where the plastic "HEATHKIT" emblem is affixed. The two fastening posts will be held to the front panel by one of two types of fasteners, either a thin metal fastener resembling a lockwasher or a thicker stamped fastener resembling a common machine nut. If the nut type fastener is used on your panel, remove the right hand fastener and replace it with the fastener supplied with this package. After replacing the fastener (or if this replacement was not necessary) use a pair of wire-cutters or a hobbyknife to cut the right hand plastic post to a height of no more than 1/16" above the fastener. Replace the gray front panel on the computer. NOTE: This modification is necessary to allow the front panel to fit properly with the DG-SS1 board installed.

8) Remove the CPU card from the computer and set it aside temporarily.

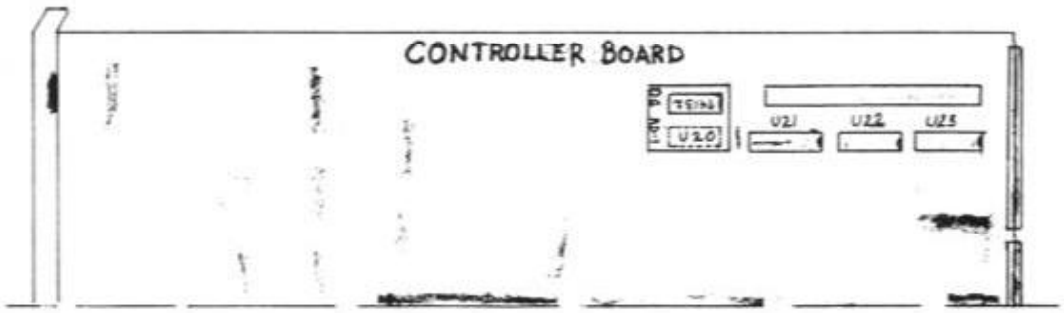
9)* Remove the disk controller board from the H8 computer.

10)* Locate U2Ø (74LS132 or 74132) and remove this IC from the disk controller board.

11)* Install the 74LS132 (74132) from step 1Ø above on the DG-RD1 circuit board as shown below:



12)* Plug the DG-RD1 circuit board into socket U2Ø on the disk controller board as illustrated below. Orient the board such that the writing faces the heat sink bracket. The 74LS132 (74132) will appear upside-down as it did when it was removed.



13)* Locate U14 (Heath part #444-19) on the disk controller circuit board and carefully remove the ROM. Plug this ROM into socket U11 on the DG-8Ø Z8Ø CPU board. BE SURE THAT PIN 1 (MARKED BY A SMALL DOT AT THE NOTCHED END OF THE ROM) IS LOCATED AT THE PIN 1 POSITION OF THE SOCKET!!

14)* If you plan to operate your system at a system clock frequency of 4 MHz, refer to the DG-ADP4 instructions for installation of this adapter. Otherwise, reinstall the disk controller board in the H8 mainframe.

15) Locate the DG-FPM/8Ø ROM in the FP8 package and install this ROM at U1Ø on the DG-8Ø CPU board. The notched end of the ROM should be TOWARD the edge connector.

16) Refer to the DG-8Ø instruction manual for switch and jumper descriptions. Set the following switches and jumpers on the board:

Jumper "A" (U1Ø)	18 TO CS 19 TO A1Ø 21 TO +5
Jumper "B" (U11)	18 TO CS 19 TO A1Ø 21 TO +5
MEM SPACE¶	ØK,1K,2K,3K 'ON' ALL OTHERS OPEN ('OFF')
J9	1K JUMPED TO "A" 2K,3K JUMPED TO "B"

¶If the disk system in NOT being used, then the 2K and 3K switches should be OPEN ('OFF').

17) Refer to the "MEMORY CONSIDERATIONS" section of this manual for a discussion of various system configurations and using this information set the 'MEM ADDR' and 'WAIT ADDR' switches on the DG-8Ø CPU for YOUR configuration.

18) Install the DG-8Ø CPU in your H8 computer being careful to orient pin 1 of P/S 2Ø1 properly.

19) Locate the keytop stickers in the FP8 package and install these as shown in the figure on page 6.

20) Plug in the computer and turn the power switch to "ON". The computer should 'beep' and come on in the monitor mode. The display should show the PC contents as ØØ4 365. If this is not the case, turn off the computer and recheck the installation procedure.

21) Turn off the computer. Replace the tie bracket and top cover of the computer. Installation of the DG-FP8 package is now complete.

APPENDIX A: MEMORY CONSIDERATIONS

The DG-FP8 hardware/firmware package is compatible with many memory configurations. The absolute minimum configuration would utilize 16K of RAM running from ØK to 16K and no ROM disable port. FPM/8Ø would occupy 1792 bytes of RAM beginning at ØK as well as use the first 64 bytes of RAM beginning at 8K (Ø4Ø ØØØ). This system would operate with the Heath cassette system but would not provide enough free RAM for operation with the H17 disk system. In this case, the CPU on-board MEM ADDR switch would be set to occupy some space above 16K. (Remember, the necessary CPU ROM information is transferred from the CPU on-board ROM to low RAM during system initialization.)

The DG-FP8 may be used with up to 56K of system RAM without using a ROM disable port. In this case, the ROM on the CPU board should be addressed at the first available 8K block above the system RAM. For example, if 56K of system RAM was being used, this RAM would occupy the space from ØK up to 56K, and the MEM ADDR switch on the DG-8Ø CPU would be set at 56K. This system would allow 48K of usable RAM when running HDOS or 56K of usable RAM when running CP/M.

The usable system RAM space may be expanded by using a ROM disable port such as the DG-CMD1.* The SYSINIT program contained in the DG-FP8 package will turn off the CPU memory using this device allowing 64K of RAM in the computer.¶ Thus 56K of RAM may be used under HDOS or 64K of RAM may be used under CP/M. If a ROM disable port other than the DG-CMD1 is used, it must be addressable at I/O address Ø77 octal and capable of interpretting a logic "1"

on data bus bit D7 as "ROM DISABLE TRUE".

The DG-64D 64K memory board offers the simplest system for use with the FP8 package. A ROM disable port is available on the DG-64D and is fully compatible with the DG-FP8. During SYSINIT, the CPU memory will be disabled using the DG-64D on-board ROM disable port and the full 64K of RAM on the board will be enabled. In this case, the MEM ADDR switch on the DG-8Ø should be set at 48K and the B3 (block 3) switch on the DG-64D should be set to 'OFF'. For further information on this mode of system operation, see the DG-64D Operations Manual.

WAIT STATES

Wait states should not be required when operating the system at 2.048 MHz using standard memory boards available. If the system will be operated at 4 MHz, the DG-64D may be used with NO wait states. Other memory boards may require the insertion of wait states for 4 MHz operation and this may be accomplished using the WAIT ADDR switch on the DG-8Ø CPU. Refer to the DG-8Ø CPU Operation Manual for information on the use of wait states to utilize slower memory in the system.

*WARNING: A modification to your DG-8Ø CPU may be necessary for this mode of operation. See Appendix C.

¶ A patch MUST be installed in the HDOS to run the system with 64K of RAM. See Appendix B for information on this patch.

APPENDIX B: SYSTEM PATCHES

The following HDOS system patches may be installed using the "Patch" program (Patch.ABS) provided on the Heath distribution diskette and may only be used with HDOS Ver. 1.6.

The symbols used in the instructions are given in the following format:

[CR] CARRIAGE RETURN
[CTRL D] SYMBOL FOR CONTROL "D" SEQUENCE.

Underlined text is used to indicate operator input from the console. The patch listing will give the display you will see on the console. All underlined characters are to be entered by the user. Note, XXX refers to a quantity which will not be altered by the user.

DO NOT ATTEMPT TO PATCH YOUR DISTRIBUTION DISKETTE!!

HDOS MEMORY SIZING PATCH

HDOS was originally designed to operate in a system using ROM (Read Only Memory) somewhere in the memory space. This patch will allow HDOS to operate with 64K of RAM (Random Access Memory) yet still properly determine the usable memory space. You should begin with a bootable diskette which contains the patch program (Patch.ABS). After booting the diskette proceed through the following steps. If you make an error, the patch program will tell you to restart the procedure. The diskette will not actually be patched until all of the following steps have been completed successfully.

```
>PATCH                    [CR]
PATCH ISSUE # 50.05.00
FILE NAME?  HDOS.SYS    [CR]
PATCH ID?  IEGJIH       [CR]
PREREQUISITE CODE? IFBEIADPGEFFCF  [CR]
ADDRESS? 2271  [CR]
002271=XXX/    [CR]
002272=XXX/    [CTRL D]
ADDRESS? 24    [CR]
000024=061/315 [CR]
000025=200/376 [CR]
000026=042/054 [CR]
000027=XXX/    [CTRL D]
ADDRESS? 211   [CR]
000211=041/041 [CR]
000212=227/000 [CR]
000213=047/050 [CR]
000214=056/044 [CR]
000215=000/050 [CR]
000216=044/007 [CR]
000217=176/176 [CR]
000220=064/064 [CR]
000221=276/276 [CR]
000222=167/167 [CR]
000223=302/302 [CR]
000224=216/214 [CR]
000225=047/047 [CR]
000226=XXX/    [CTRL D]
ADDRESS? 5372  [CR]
005372=054/212 [CR]
005373=040/303 [CR]
005374=157/205 [CR]
005375=162/053 [CR]
005376=040/341 [CR]
```

```
005377=106/061 [CR]
006000=151/200 [CR]
006001=154/042 [CR]
006002=145/345 [CR]
006003=163/076 [CR]
006004=040/177 [CR]
006005=104/074 [CR]
006006=141/350 [CR]
006007=155/041 [CR]
006010=141/000 [CR]
006011=147/000 [CR]
006012=145/042 [CR]
006013=144/215 [CR]
006014=056/047 [CR]
006015=212/311 [CR]
006016=303/000 [CR]
006017=205/000 [CR]
006020=053/000 [CR]
006021=XXX/     [CTRL D]
ADDRESS?        [CTRL D]
PATCH CHECK CODE? BEEBOHMF
PATCH ISSUE # 50.05.00
FILE NAME?      [CTRL D]
>
THE FILE HAS NOW BEEN PROPERLY PATCHED.
```

SPACES HAVE BEEN INSERTED TO ENHANCE READABILITY BUT SHOULD NOT BE USED WHEN MAKING ENTRIES!

DRIVE SPEED TEST PATCH

This patch may be used to adapt the HDOS drive speed test for use with systems operating at a 4 MHz clock frequency. You should begin with a bootable diskette containing the patch program (Patch.ABS). After booting the diskette, proceed through the following steps. If you make an error, the patch program will tell you to restart the procedure. The diskette will not actually be patched until all of the following steps have been completed successfully.

```
Boot the system and type PATCH
>PATCH                    [CR]
PATCH ISSUE # 50.05.00
FILE NAME?  TEST.ABS      [CR]
PATCH ID?  KHOJEO         [CR]
PREREQUISITE CODE?  IFBEIADPGEFFCF  [CR]
ADDRESS? 45136      [CR]
045136=041/315      [CR]
045137=233/367      [CR]
045140=045/066      [CR]
045141=XXX/         [CTRL D]
ADDRESS? 66367      [CR]
066367=040/041      [CR]
066370=103/233      [CR]
066371=117/045      [CR]
066372=056/247      [CR]
066373=054/170      [CR]
066374=040/037      [CR]
066375=061/107      [CR]
066376=071/171      [CR]
066377=067/037      [CR]
067000=071/117      [CR]
067001=012/311      [CR]
067002=XXX/         [CTRL D]
ADDRESS? 55346      [CR]
055346=050/064      [CR]
055347=060/132      [CR]
055350=XXX/         [CR]
ADDRESS?            [CTRL D]
PATCH CHECK CODE?  LECCCGIF
PATCH ISSUE # 50.05.00
FILE NAME?          [CTRL D]
>
The file has now been properly patched.
SPACES HAVE BEEN INSERTED TO ENHANCE READABILITY BUT SHOULD NOT
BE USED WHEN MAKING ENTRIES!
```

APPENDIX C: DG-8Ø & ROM DISABLE CONSIDERATIONS

In order to utilize RAM in the full 64K memory space of the H8 computer, a ROM disable port must be used. Furthermore, care must be taken to insure that the CPU data bus output buffers are not active at the same time that memory board buffers are attempting to place data on the bus. DG-8Ø CPU's with serial numbers 118904031 or 123708025 and greater have been modified to assure that this data bus contention will not occur and no modification is required. However, DG-8Ø's with the following serial numbers must be modified as follows for proper operation with a ROM disable port such as the DG-CMD1. Please note that this modification is not required if your system incorporates the DG-64D bank-select memory board with the FP8 monitor package.

SERIAL NUMBERS: 112604000 through 118804030
115608000 through 123608024

On the Heath 8Ø8Ø CPU board for the Heath H8, jumper 'K' allows the user to determine if the data bus buffers are active during on-board memory access or disabled. The DG-8Ø operates in the manner of the Heath CPU when Heath jumpers 'K_1' and 'K_2' are shorted. In this mode, the data bus buffers are active during on-board memory access. The following simple modification may be made to the DG-8Ø to allow the buffers to be disabled during on-board memory access:

1) Place the DG-8Ø before you with the component side up and the edge-connector to the right.

2) Near the lower center of the board, locate the solder pad immediately below and between the silkscreened © symbol and the '1980' symbol.

3) On the component side of the board, cut the trace that runs from this solder pad toward the edge-connector. (This trace turns toward the top of the board about ¼" from the solder pad.)

4) Locate U13 on the CPU board and determine pin 8 of this IC.

5) Turn the board over to the solder side and again carefully locate pin 8 of U13.

6) Solder a wire jumper from pin 8 of U13 to the pad located in step 2. Run this jumper on the solder side of the board.

7) Recheck your work and then install the CPU board and check for proper operation.

WARRANTY

NO WARRANTY EXPRESSED OR IMPLIED IS ASSOCIATED WITH THIS PRODUCT EXCEPT FOR THE WARRANTY THAT THE GOODS ARE PRODUCED IN A PROFESSIONAL MANNER AND IN ACCORDANCE WITH THE SPECIFICATIONS SUPPLIED. DG ELECTRONIC DEVELOPMENTS CO. SHALL NOT BE LIABLE FOR ANY INJURY, LOSS OR DAMAGE, DIRECT OR CONSEQUENTIAL ARISING OUT OF THE USE OF OR THE INABILITY TO USE THIS PRODUCT.

FPM/8Ø REAL-TIME CLOCK DEMONSTRATION

The following program was included as a demonstration of the FPM/8Ø Real-Time Clock. This program may be assembled using the Heath assembler (ASM.ABS) and must be used with the FPM/8Ø monitor.

DG-FP8 ADDENDUM

DRIVE SPEED TEST PATCH

This patch may be used to adapt the HDOS drive speed test for use with systems operating at a 4 MHz clock frequency. You should begin with a bootable diskette containing the patch program (Patch.ABS). After booting the diskette, proceed through the following steps. If you make an error, the patch program will tell you to restart the procedure. The diskette will not actually be patched until all of the following steps have been completed successfully.

```
Boot the system and type PATCH
>PATCH                          [CR]
PATCH ISSUE # 50.05.00
FILE NAME?  TEST.ABS    [CR]
PATCH ID?  KHOJEO       [CR]
PREREQUISITE CODE?  IFBEIADPGEFFCF    [CR]
ADDRESS?  45136    [CR]
045136=041/315     [CR]
045137=233/367     [CR]
045140=045/066     [CR]
045141=XXX/        [CTRL D]
ADDRESS?  66367    [CR]
066367=040/041     [CR]
066370=103/233     [CR]
066371=117/045     [CR]
066372=056/247     [CR]
066373=054/170     [CR]
066374=040/037     [CR]
066375=061/107     [CR]
066376=071/171     [CR]
066377=067/037     [CR]
067000=071/117     [CR]
067001=012/311     [CR]
067002=XXX/        [CTRL D]
ADDRESS?  55346    [CR]
055346=060/064     [CR]
055347=060/132     [CR]
055350=XXX/        [CTRL D]
ADDRESS?           [CTRL D]
PATCH CHECK CODE?  LECCGIF
PATCH ISSUE # 50.05.00
FILE NAME?         [CTRL D]
>
```

The file has now been properly patched.

SPACES HAVE BEEN INSERTED TO ENHANCE READABILITY BUT SHOULD NOT BE USED WHEN MAKING ENTRIES!

APPENDIX C: DG-8Ø & ROM DISABLE CONSIDERATIONS

In order to utilize RAM in the full 64K memory space of the H8 computer, a ROM disable port must be used. Furthermore, care must be taken to insure that the CPU data bus output buffers are not active at the same time that memory board buffers are attempting to place data on the bus. DG-8Ø CPU's with serial numbers 118904031 or 123708025 and greater have been modified to assure that this data bus contention will not occur and no modification is required. However, DG-8Ø's with the following serial numbers must be modified as follows for proper operation with a ROM disable port such as the DG-CMD1. Please note that this modification is not required if your system incorporates the DG-64D bank-select memory board with the FP8 monitor package.

SERIAL NUMBERS: 112604000 through 118804030
115608000 through 123608024

On the Heath 8Ø8Ø CPU board for the Heath H8, jumper 'K' allows the user to determine if the data bus buffers are active during on-board memory access or disabled. The DG-8Ø operates in the manner of the Heath CPU when Heath jumpers 'K_1' and 'K_2' are shorted. In this mode, the data bus buffers are active during on-board memory access. The following simple modification may be made to the DG-8Ø to allow the buffers to be disabled during on-board memory access:

1) Place the DG-8Ø before you with the component side up and the edge-connector to the right.

2) Near the lower center of the board, locate the solder pad immediately below and between the silkscreened © symbol and the '1980' symbol.

3) On the component side of the board, cut the trace that runs from this solder pad toward the edge-connector. (This trace turns toward the top of the board about ¼" from the solder pad.)

4) Locate U13 on the CPU board and determine pin 8 of this IC.

5) Turn the board over to the solder side and again carefully locate pin 8 of U13.

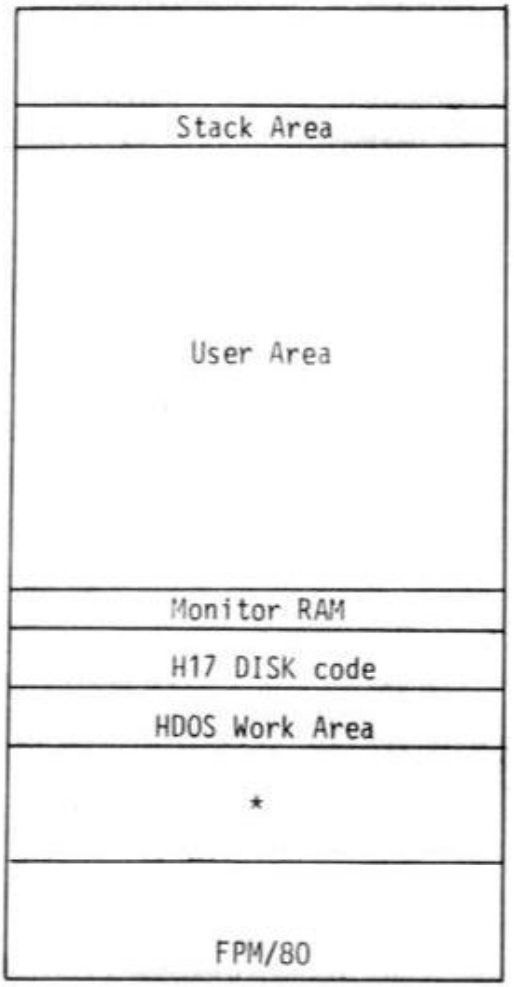
6) Solder a wire jumper from pin 8 of U13 to the pad located in step 2. Run this jumper on the solder side of the board.

7) Recheck your work and then install the CPU board and check for proper operation.

APPENDIX D

FPM/80 Memory Map

This memory map reflects usage after SYSINIT has transferred ROM code into RAM and disabled the CPU on-board ROM. Therefore the entire occupied address space is made up of RAM.



End of Address Space (64K)

Stack begins at upper boundary of RAM and will use a maximum of 120_8 (80_{10}) bytes under FPM/80.

040 100 64 Bytes

040 000 2K Bytes

030 000 1K Bytes

024 000

010 000

2048 Bytes

000 000

*Care should be used when utilizing this RAM space as future DG or Heath products may occupy portions of this RAM.

APPENDIX E: HEATH SOFTWARE PATCHES

The following Heath/Microsoft software products for CP/M require simple patches to operate properly on systems incorporating the DG-FP8 monitor package and/or the DG/Magnolia version of CP/M. The user should first transfer the file to be patched onto a diskette he plans to use as his "system" diskette.

WARNING: DO NOT ATTEMPT TO PATCH THE SOFTWARE DISTRIBUTION DISKETTE!!

The system should then be booted and the indicated file patched using DDT as outlined below. All console output is shown in these procedures with user input underlined for clarity. Note that a carriage return (RETURN) should be pressed after each full line of user input.

PATCH FOR MICROSOFT BASIC VERSION 4.83

Patch the file MBASIC.COM as follows:

```
A>DDT MBASIC.COM
DDT VERS 2.2
NEXT  PC
4F00 0100
-F4D3A,4D8D,0
-F3DAA,3DD0,0
-G0

A>SAVE 79 MBASIC.COM

A>
```

This patch is now complete.

PATCH FOR MICROSOFT BASIC VERSION 5.21:

Patch the file MBASIC.COM as follows:

```
A>DDT MBASIC.COM
DDT VERS 2.2
NEXT  PC
6100 0100
-F5F08,5F5B,0
-F4793,47B9,0
-G0

A>SAVE 97 MBASIC.COM

A>
```

This patch is now complete.

PATCH FOR MICROSOFT BASIC COMPILER:

Patch the file BASCOM.COM as follows:

```
A>DDT BASCOM.COM
DDT VERS 2.2
NEXT  PC
7D00 0100
-S400C
400C C1 00
400D C4 .
-A412A
412A  JMP 4151
412D  .
-G0

A>SAVE 125 BASCOM.COM

A>
```

This patch is now complete.

MICROSOFT COBOL-8Ø VERSION 4.01:

Patch the file COBOL.COM as follows:

```
A>DDT COBOL.COM
DDT VERS 2.2
NEXT  PC
7200 0100
-F6199,61F0,0
-G0

A>SAVE 114 COBOL.COM

A>
```

This patch is now complete.

MICROSOFT M8Ø ASSEMBLER:

This patch is only required for M8Ø as distributed with the Microsoft COBOL-8Ø package. Patch the file M8Ø.COM as follows:

```
A>DDT M8Ø.COM
DDT VERS 2.2
NEXT  PC
4C00 0100
-F4392,43E9,0
-G0

A>SAVE 76 M8Ø.COM

A>
```

This patch is now complete.

DG-ADP4

INSTALLATION

USER NOTES

ELECTRONIC

INTRODUCTION

The DG-ADP4 provides for operation of the Heath H17 disk system with a system clock frequency of 4 MHz. This modification is required because the H17 disk controller timing is based on the CPU clock frequency. The ADP4 modifies disk controller timing so that the H17 disk system operates properly with the DG-8Ø Z8Ø CPU at a clock frequency of 4 MHz. No special tools or skills are required for installation of the DG-ADP4 as the board simply plugs directly into IC sockets on the H17 disk controller board.

The DG-ADP4 is designed for use in conjunction with the DG-8Ø CPU and requires the use of the DG-FP8 hardware/firmware support package. These components along with the DG-64D memory board provide the H8 user with a powerful yet flexible 4 MHz Z8Ø based computer system.

DG-ADP4 OPERATION

Operation of the Heath H17 disk system with the DG-ADP4 is virtually identical to normal H17 operation. The user may notice an increase in the number of "soft" (recoverable) errors the system encounters during read/write of a diskette which was "SYS-GENED" with the system operating at 2 MHz. As explained in the Heath HDOS operations manual, these errors are not serious and should not effect normal system operation.

DG-ADP4 INSTALLATION

Ø) Turn off and unplug the H8 computer.

1) Remove the H17 disk 'Controller Board' from the computer and place the board on the table before you with the edge-connector to your right.

2) Locate U2 and U3 on the left-hand side of the disk controller board. These are both 74LS161 IC's (Heath part number 443-757).

3) Remove U2 and U3 from the disk controller board and install them on the DG-ADP4 as shown in figure 1. Be sure to identify pin 1 of these IC's and locate this pin properly during installation.

4) Install the DG-ADP4 on the disk controller board at sockets U2 and U3, being sure to carefully align the plug pins with the disk controller board sockets. The "DG-ADP4" nomenclature should be toward the heat sink/mounting bracket of the controller board. You may need to 'guide' the disk capacitor located between U2 and U3 through the slot in the ADP4 circuit board. The plugs should fit 'snugly' but not require undue force to plug-in.

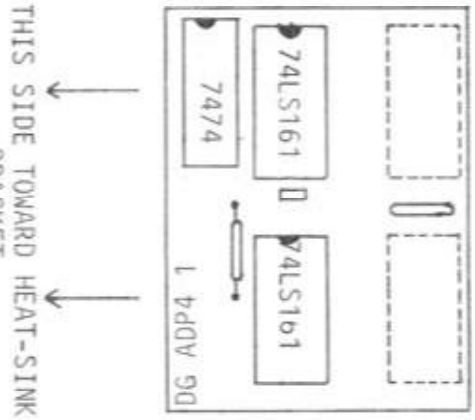
5) Set the jumpers on the DG-8Ø Z8Ø CPU board and the DG-SS1 modification board for system operation at 4 MHz. Refer to the appropriate manual for information on these jumper settings.

6) Replace the disk controller board in the H8 mainframe. If you are installing the DG-FP8 package in your system, continue with the installation instructions given in that manual. Otherwise installation of the DG-ADP4 is now complete.

7) Plug in your computer and check the system for proper operation. NOTE: The jumper in the lower left-hand

corner of the DG-ADP4 should be set to the 4 MHz position. This jumper was included to allow the user to wire an external SPDT switch to the board for remote selection of 2 or 4 MHz operation.

FIGURE 1



WARRANTY

THIS PRODUCT HAS NO WARRANTY; EXPRESSED OR IMPLIED, EXCEPT THAT IT WAS PRODUCED IN A PROFESSIONAL MANNER ACCORDING TO THE SPECIFICATIONS AND DESCRIPTION CONTAINED HEREIN. NEITHER THE SELLER NOR MANUFACTURER SHALL BE LIABLE FOR ANY INJURY, LOSS, OR DAMAGE; DIRECT OR INDIRECT, ARISING OUT OF THE USE OR INABILITY TO USE THE DG-ADP4. THE BUYER ASSUMES ALL RESPONSIBILITY IN ASCERTAINING THE SUITABILITY OF THIS PRODUCT FOR HIS INTENDED USE.

DG-8Ø ADDENDUM
March, 1981

This addendum contains update information on the use of the DG-8Ø Z8Ø CPU Board with various DG and Heath products. A new schematic for the DG-8Ø has also been included which should be useful for those persons wishing to modify or repair their board after the warranty period has lapsed.

TABLE OF CONTENTS

JUMP-ON-RESET OPERATION

The DG-8Ø CPU offers a jump-on-reset function to on-board memory addressed at any 1K byte boundary of the available memory space. This feature allows greater flexibility in the design of custom panel monitors or other types of system firmware. The following explanation should clarify the use of this function.

When a hardware reset occurs, the Z8Ø microprocessor zeroes the Program Counter and initializes the other internal registers in preparation for instruction execution. When the reset sequence ends, the CPU then fetches its first instruction from location ØØØ ØØØ octal. For this reason, program memory (ROM or PROM) is usually located at the "bottom" of the memory space in simple microcomputer systems.

The DG-8Ø includes circuitry which "forces" the NOP instruction code onto the CPU data bus when a hardware reset occurs. This NOP code remains on the bus until the on-board memory is addressed by the CPU. If the system program memory is addressed at the bottom of memory (i.e., ØØØ ØØØ octal) then the NOP is removed from the bus immediately and the CPU fetches its first instruction from ØØØ ØØØ octal. However, if the program memory is addressed at some other location higher in memory, then the CPU will execute NOP's until the program counter increments to the location of the on-board program memory where program execution will begin. The forced NOP prevents the CPU from accessing any other memory in the computer until the on-board program memory has been accessed.

The following should be kept in mind when utilizing the jump-on-reset function of the DG-8Ø:

1) The ROM or PROM containing program memory must be programmed to occupy the location at which it is addressed on the DG-8Ø. For example, PAM-8 will only operate properly if addressed at ØK on the DG-8Ø.

2) The jump-on-reset feature is not functional if the $\overline{\text{ROMDIS}}$ pin (pin 46 on the Heath Bus) is continuously held low following a system reset. In this case, the on-board memory is never accessed and program execution will begin with the random RAM contents at ØØØ ØØØ octal.

The following example illustrates the use of the Jump-On-Reset Feature:

Suppose the user wishes to use a custom 2K byte ROM monitor designed to be addressed at 2ØØ ØØØ offset octal. Since this address corresponds to 32K in decimal, the MEM ADDR switch would be set to 32K (refer to page 6 and 7 of the DG-8Ø Operation Manual for switch and jumper descriptions). The 2K byte ROM will occupy the lowest two 1K byte blocks of the 8K byte block beginning at 32K so the ØK and 1K MEM SPACE switches would be set "ON". The 1K position of jumper J9 would be set to "A" (the ØK block is always assigned to ROM socket "A") and the ROM would be plugged into ROM socket "A" (U1Ø). When the computer is turned on or a reset executed, program execution will now begin with the first instruction contained in the ROM at 32K.

DG-8Ø WITH THE HEATH "EXTENDED CONFIGURATION OPTION"

The DG-8Ø may be configured for operation with the Heath "Extended Configuration Option" by setting the following switches and jumpers. Note that one soldered jumper must be installed for compatibility with the 2532-type EPROM (Heath part number 444-74) used by Heath. A simple modification will also be required on DG-8Ø's manufactured before October, 198Ø. This modification is described in the "DG-8Ø ROM-Disable Considerations" section of this addendum.

Switch and Jumper settings are as follows (Refer to pages 6 and 7 of the DG-80 Instruction Manual for switch and jumper descriptions.):

Switch or Jumper	Setting
WAIT ADDR	All switches "OPEN"
MEM ADDR	ØK "ON", All others "OPEN"
MEM SPACE	ØK,1K,2K,3K "ON", all others "OPEN"
JUMPER J9	1K,2K,3K set to "A"
JUMPER "A"	Pin 19 set to "A1Ø"
	Pin 21 set to "+5V"
	Pin 18 - see below
JUMPER "B"	No jumpers installed

Pin 18 of jumper "A" must be connected to CPU address Bit "A11". This may be accomplished by running a jumper on the SOLDERED SIDE of the board as shown in Figure 1. Carefully inspect your DG-80 before installing this jumper to insure that you connect the pads indicated in the figure.

All remaining DG-8Ø jumpers should be set as distributed from the factory.

Switch settings of the Heath Extended Configuration Board and Operation of H8 Computer are now as described in the Heath HAS-8 and XCON-8 Manuals.

OPERATION OF THE DG-8Ø WITH THE HEATH WH8-16 16K MEMORY BOARD

Two versions of the Heath WH8-16 16K memory board have been produced. These versions of the board may be identified by the Heath part number, 85-XXXX. The later version of the board (Part Number 85-2197) is fully compatible with the DG-8Ø CPU, however; the earlier version (Part Number 85-2Ø97) requires a simple modification to operate properly with the DG-8Ø. The following explanation and modification is provided for owners of the earlier version of the WH8-16.

The early Heath WH8-16 memory board was designed for use with the Heath 8Ø8ØA using the 8238 type system controller. This system controller provides an "advanced" memory write signal with a duration of about 115Ø ns. Since only 45Ø ns is required to access the memory on the WH8-16 this memory write signal is delayed on the memory board to reduce the time the memories are selected and thus reduce the power dissipation of the board.

The Z8ØA microprocessor does not provide the advanced memory write feature of the 8Ø8ØA-8238 combination. Using a 2.Ø48 MHz clock the memory write signal from the Z80 CPU has a duration of approximately 488 ns which is adequate for memory access but does not waste power by prolonging the access. If the Z8Ø is used with the early WH8-16 in its standard configuration the delay present on the memory board will prevent memory access during write and the board will fail to function properly.

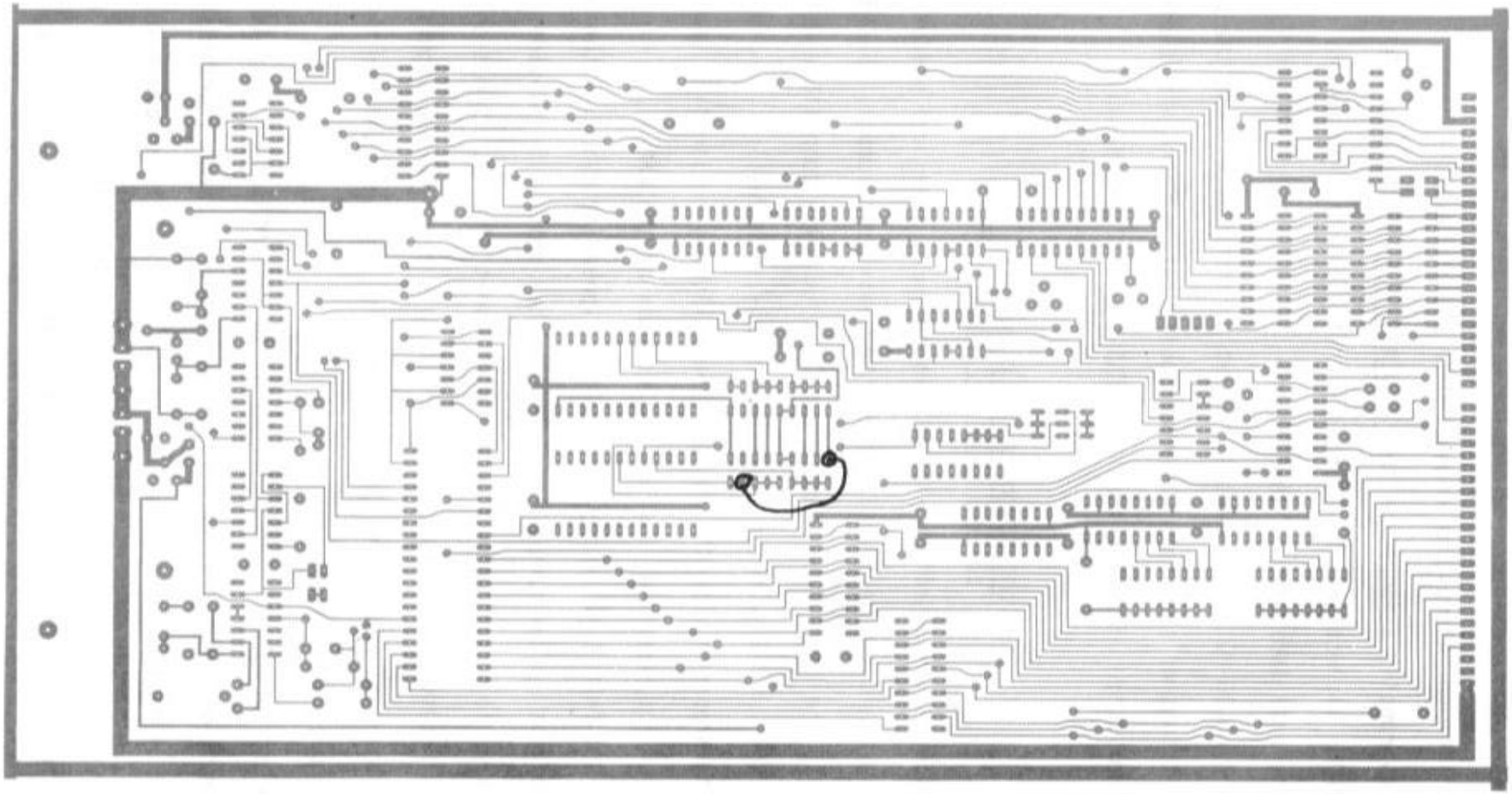


FIGURE ONE: HEATH EXTENDED CONFIGURATION ROM MODIFICATION FOR THE DG-8Ø CPU.

In order to alleviate the above problem the following simple modification can be made to your WH8-16 board. Remember, this modification is only necessary on the early version (Part Number 85-2Ø97) of the WH8-16.

1) On the component side of the board locate U142, a 74LS74 dual "D" flip-flop.

2) Carefully determine pin 11 of U142 and make a small cut in the foil leading to this pin. This cut should be approximately 1/16" in width and far enough from U142 so that a jumper may be soldered across it if you should ever wish to return your board to its original configuration.

3) Turn the board over to the soldered side and again locate U142.

4) Carefully determine pin 3 and pin 11 of U142. Remember you are now looking at the IC from the bottom, so be sure to start counting at the correct position.

5) Using insulated wire solder a short jumper from pin 3 to pin 11 of U142. Be sure that no foils are bridged when the jumper is in place and that the jumper itself does not short to any other foils.

6) BE SURE TO DOUBLE CHECK YOUR WORK!

7) The board is now ready for operation with a Z8ØA microprocessor.

NOTE: This configuration is compatible with the 8Ø8ØA CPU but the power dissipation of the board will be slightly higher.

NO LIABILITY IS ASSUMED BY D-G ELECTRONIC DEVELOPMENTS COMPANY FOR USER MODIFICATIONS TO THEIR OWN SYSTEMS.

APPENDIX C: DG-8Ø & ROM DISABLE CONSIDERATIONS

In order to utilize RAM in the full 64K memory space of the H8 computer, a ROM disable port must be used. Furthermore, care must be taken to insure that the CPU data bus output buffers are not active at the same time that memory board buffers are attempting to place data on the bus. DG-8Ø CPU's with serial numbers 1189Ø4Ø31 or 1237Ø8Ø25 and greater have been modified to assure that this data bus contention will not occur and no modification is required. However, DG-8Ø's with the following serial numbers must be modified as follows for proper opera-

tion with a ROM disable port such as the DG-CMD1. Please note that this modification is not required if your system incorporates the DG-64D bank-select memory board with the FP8 monitor package.

SERIAL NUMBERS: 1126Ø4ØØØ through 118Ø4Ø3Ø
115608ØØØ through 123608Ø24

On the Heath 8Ø8Ø CPU board for the Heath H8, jumper "K" allows the user to determine if the data bus buffers are active during on-board memory access or disabled. The DG-8Ø operates in the manner of the Heath CPU when Heath jumpers "K_1" and "K_2" are shorted. In this mode, the data bus buffers are active during on-board memory access. The following simple modification may be made to the DG-8Ø to allow the buffers to be disabled during on-board memory access:

1) Place the DG-8Ø before you with the component side up and the edge-connector to the right.

2) Near the lower center of the board, locate the solder pad immediately below and between the silkscreened © symbol and the "198Ø" symbol.

3) On the component side of the board, cut the trace that runs from this solder pad toward the edge-connector. (This trace turns toward the top of the board about ¼" from the solder pad.)

4) Locate U13 on the CPU board and determine pin 8 of this IC.

5) Turn the board over to the solder side and again carefully locate pin 8 of U13.

6) Solder a wire jumper from pin 8 of U13 to the pad located in step 2. Run this jumper on the solder side of the board.

7) Recheck your work and then install the CPU board and check for proper operation.

D·G

SYSTEM ENHANCEMENTS FOR THE HEATH® H8 COMPUTER

DG-80 ZILOG Z80 CPU

FEATURES

• Compatible with Heath* H8 hardware and software • Z80 CPU—Enhanced instruction set • Provisions for up to 8K ROM/EPROM and/or 4K RAM • Jump-On-Reset to any 1K boundary • Operational up to 4 MHz (2.048 MHz standard) • DIP switch selectable wait states for any or all 8K blocks of memory • All Z80 interrupt response modes available • Interrupt Acknowledge and Dynamic Memory Refresh signals available on bus • Frequently selected options by DIP switch or solderless jumper • Machined contact gold sockets for ROM/EPROM, RAM • Includes many advanced features for future expansion • Assembled, tested and guaranteed • Extensive operations manual and Z80 PROGRAMMING MANUAL.

GENERAL

DG Electronic Development Co. conceives a new generation CPU delivering power, speed, and flexibility never before possible for the Heath* H8 microcomputer. The DG-80, utilizing the powerful Z80 microprocessor aids the user in developing the H8's true potential and provides for future expansion. Significant advancements in 8 bit microprocessor architecture, coupled with the Z80's expanded and powerful instruction set, offers outstanding performance, yet maintains compatibility with your current system hardware and software.

The DG-80 CPU opens a new library of available software. The JUMP-ON-RESET feature allows restarting of program ROM on any 1K boundary of the 64K memory space. This provides for RAM in low memory as is the convention in many of the popular S-100 systems.

The DG-80 offers operation speeds up to 4 MHz with DIP switch selectable wait states available for any or all 8K blocks of memory. This feature allows full advantage to be taken of high speed memory boards without obsoleting slower memory.

The RESET function has been configured such that systems using dynamic memory will preserve memory contents during RESET. Another option, which places the RFS signal on the bus, allows use of HALT instructions while utilizing the Z80's intrinsic refresh capability.

Much of the flexibility designed into the DG-80 offers itself to applications of the H8 computer in the commerical industrial, educational, and scientific communities. Coupled with the DG-FP8 and the DG-ADP4, the DG-80 allows the hobbyist and the professional for the first time to make his choices as to hardware, firmware, and software support.

DG-80 Zilog Z80 CPU **$249.00**

DG-ADP4

The DG-ADP4 provides for operation of the Heath H17 disk system with a system clock frequency of 4 MHz. This modification is required because the H17 disk controller timing is based on the CPU clock frequency. The ADP4 modifies disk controller timing so that the H17 disk system operates properly with the DG-80 Z80 CPU at a clock frequency of 4MHz. No special tools or skills are required for installation of the DG-ADP4 as the board simply plugs directly into IC sockets on the H17 disk controller board.

The DG-ADP4 is designed for use in conjunction with the DG-80 CPU and requires the use of the DG-FP8 hardware/firmware support package. These components along with the DG-64D memory board provide the Heath* H8 user with a powerful yet flexible 4MHz Z80 based computer system.

DG-ADP4 **$19.95**

DG-FP8 NEW MONITOR SUPPORTS STANDARD CP/M AND HDOS FOR THE H8

The DG-FP8 gives the user the full scope of the present PAM-8* panel monitor, including single-step, plus added features to make full use of the DG-80.

The DG-FP8 is an easily installed hardware/firmware package offering many advanced features including automatic determination and system configuration on boot-up for HDOS or standard CP/M operation.

GENERAL FEATURES

• PAM* Compatible monitor designed to operate from RAM in low memory • Maintains entry points to all PAM-8* routines including cassette routines • Split octal or hexadecimal display & entry • Two keystroke display of memory contents pointed to by any register • Automatically sets PC register to boot routine address on power-up • Real time clock

Z80 MONITOR FEATURES

• Displays and alters contents of primary and alternate registers • Displays and alters IX and IY index registers (used for index addressing) • Provisions for non-maskable interrupt entry • Allows operation of Panel Monitor in Z80 alternate interrupt modes • Displays and alters interrupt vector register • Provides for PAM-8* type single-step using the Z80 microprocessor

ADDITIONAL FEATURES

• Provides 4MHz software support for H17 disk system using DG-ADP4 hardware conversion • Supports standard CP/M Ver. 2.2 as well as HDOS • Fully documented source listing included • Necessary hardware conversion for Heath* front panel is provided (no soldering or special skills required for installation) • This package is designed primarily for advanced operation of the DG-80 CPU with the H17 disk system, but is fully compatible with the Heath tape system.

DG-FP8	(Documentation Only — $15.00 Source listing not included.)	$69.95

DG-32D DYNAMIC RAM

FEATURES

• Fully compatible with all current Heath* hardware and software • Conveniently arranged as four independently addressable 8K Byte blocks • Simple memory addressing by use of two 8-position DIP switches • Uses popular 4116 type RAM devices • Transparent on-board refresh requiring no wait states • Typical power consumption of less than 6 watts • Fully assembled, tested, and "burned-in" • Guaranteed for 90 days

32K	$339.00
16K	$287.00
ØK	$233.00
Documentation only	$15.00

DG-64D DYNAMIC RAM

FEATURES

• Up to 64K bytes capacity Dynamic RAM • Hardware bank selectable in 8K increments • Software bank selectable in 16K increments through I/O port • On-board bank select/CPU ROM disable port, addressable to any 256 I/O addresses • Up to 8 boards controllable through one I/O port (allows page mode operation) • On-board transparent refresh for 8080 or Z80 microprocessor backed up by asynchronous refresh upon loss of normal program execution • Low power consumption — less than 8 watts • Assembled, tested & burned in — 90 day warranty.

GENERAL

The DG-64D is a high technology 64K byte dynamic random access memory for use with Heath* H8 computers. The many features incorporated in the DG-64D make it the most flexible and powerful memory available for the Heath* H8. Low power requirements (less than 8 watts) permit utilization of 64K (or more!) of memory while allowing a full compliment of other peripherals.

The DG-64D Bank Select feature allows several 64K boards to be operated in one computer with the total memory space divided into 16K "pages". Thus systems may be programmed to use RAM, for fast, transient storage areas and avoid using slower disk or tape for that function.

DG-64D	$529.00
48K	$480.00
32K	$431.00
16K	$382.00
8K	$333.00
Documentation Only	$15.00

DG-CMD1

ROM disable port for use with the Heath* H8 computer. Addressable to any of 256 I/O ports. Allows the use of a full 64K of RAM when used in conjunction with the DG-80 CPU and the DG-FP8 hardware/firmware package (NOT REQUIRED FOR SYSTEMS UTILIZING THE DG-64D MEMORY BOARD)

DG-CMD1	$29.95

STANDARD CP/M NOW AVAILABLE FOR THE H8

DG Electronic Developments Co. now has available standard CP/M Ver. 2.2 for the Heath* H8 computer. The DG/Magnolia Microsystems version of standard CP/M will allow the user of H8 computers to utilize all CP/M compatible software available on Heath* formatted disks.

Standard CP/M opens new horizons of software including powerful new languages, assemblers, disassemblers, and debuggers. This CP/M may be used only in conjunction with our DG-80 Zilog Z80 based CPU and the DG-FP8 hardware/firmware monitor package.

The DG total system enhancement allows user operations under HDOS or standard CP/M software thus combining Heath* system compatibility with an additional magnitude of power and versatility.

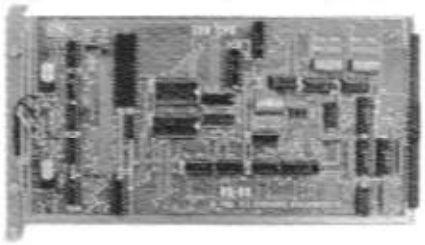
Standard CP/M Ver. 2.2 **$130.00**

THE DG ENHANCED H8 COMPUTER

DG Electronic Developments Company now has available for the Heath* H8 computer a "STANDARD" system configuration. The use of the DG-80 CPU combined with our firmware and hardware support allows the H8 owner to run a full 64K complement of memory at 2 or 4 MHz with the powerful Zilog Z80 microprocessor.

The H8 owner now has several options available. He may run under the standard Heath* configuration with HDOS at 2 or 4 MHz, utilizing the library of software owned or available for HDOS. This avoids the "scrapping" of an already sizeable investment. The second option available; which pushes the Heath* H8 into an advanced class, is utilization of standard CP/M Ver. 2.2. The advantages associated with this operating system are its "industry-wide" acceptance and the tremendous amount of software available. Of course, all software available on Heath* formatted disks, including all Z80 based software is available to the user with the DG "SYSTEM".

This powerful CPU-coupled with our DG-64D memory board with its many features finally allows the H8 owner to pursue the paths he desires without abandoning his current library of software.

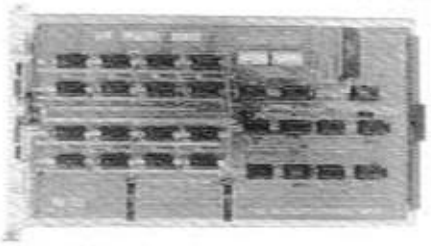


DG-80 Zilog Z80 CPU

SPECIFICATIONS

Microprocessor	Z80A (158 instructions including all 8080A instructions)
Computer Interface	Modified Heath* H50 Bus-All inputs 1 TTL load or less: Output Buffers-74LS240
Clock—Standard	2.048 MHZ
—Optional	Up to 4.0 MHz
Interrupts—Standard	Seven-Priority Vectored
—Optional	Z80 MODE 1 or MODE 2
On Board Memory	2 on-board sockets allow up to 8K ROM—EPROM or up to 4K RAM
Sockets	All IC's socketed
Switches	All frequently changed options determined solderless jumpers or DIP switches
Power Requirements—	+ 7◗ −12 VDC at 540 mA
(Note 1)	+14◗ +20 VDC at 50 mA
	−14◗ −20 VDC at 30 mA
Manuals and Documentation	Includes extensive instruction manual and Mostek* Z80 PROGRAMMING MANUAL

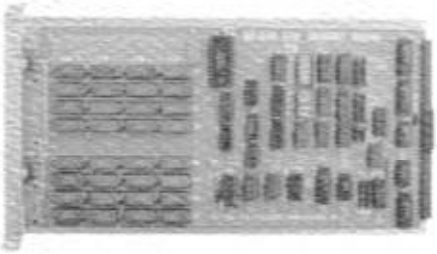
NOTES: 1-Currents given are typical with Heath* PAM-8 ROM (2308) on board and may vary according to RAM, EPROM or ROM used. The DG-80 does not include the PAM-8* ROM.



DG-32D Dynamic RAM

SPECIFICATIONS

Organization	Four independently addressable 8K Byte blocks
Address Selection	DIP Switches
Access Time	320 ns (Typical)
Interface	Heath* H8 Bus Compatible All inputs 1 TTL load or less Output Buffer—74LS240
Sockets	All I.C.'s socketed
Power Requirements	+14◗ 20 VDC at 100 mA
	+ 7◗ 12 VDC at 400 mA
	−14◗ 20 VDC at 15 mA



DG-64D Dynamic RAM

SPECIFICATIONS

Organization	64K Bytes Hardware Selectable in 8K Byte Blocks Software Selectable in 16K Byte Blocks (Hardware deselect overrides software select)
Address Selection	Hardware — Dipswitch Software — I/O Port
Access Time	240 ns (Typical)
Interface	Heath* H8 Bus Compatible All inputs 1 TTL load or less
I/O Port Selection	Any of the 256 available I/O Ports selected by solderless jumper
Refresh	On-board 8080A or Z80A compatible refresh backed up by assynchronous refresh — Also operates with DG-80 Z80-type refresh
Sockets	All I.C.'s socketed
Power Requirements	+ 14 ♦ 20 VDC @ 120 mA + 7 ♦ 14 VDC @ 400 mA − 14 ♦ 20 VDC @ 20 mA (Typical values at clock frequency of 2.048 Mhz.)

DG-ADP4

4 MHz adapter for H17 Disk System $19.95

DG-FP8

Z80 Monitor Package $69.95

DG-CMD-1

ROM Disable Port $29.95

CP/M Ver. 2.2

Standard CP/M Operating System $130.00

ADP4/FP8

Combination Purchased Together $79.95

16K MEMORY CHIPSETS

(8-4116 Type Dynamic RAMS) for DG-32D, DG-64D, Apple*, TRS-80*, H88/89*, and Pet* $49.00

D-G Electronic Developments Company was founded by three Heath users involved in high technology endeavors. These individuals recognized early in the evolution of microcomputer mainframes the flexibility of the H8 bus structure as well as the potential of the H8 system. Realizing that the dynamic technology of today allows improvements to even the best of products. D-G began development of a series of advanced, yet reasonably priced enhancements for the Heath H8 computer. To avoid the compatibility "nightmares" encountered by many microcomputer users, DG strives to maintain compatibility with all Heath H8 products.

DG desires to give the Heath H8 user the best, most technically advanced products possible. As Heath users well know, factory support is an important factor in the usefulness of the product. DG is proud that all design and software support personnel are intimately familiar with Heath H8 products and the relationship with the DG enhancements.

We know that you will find that working with the enhanced H8 system will give you power, flexibility and options that you have desired. Let DG help you bring your H8 to the current level of technology.

Ordering Information: Products and manuals are available from DG Electronic Developments Co., P.O. Box 1124, 1827 South Armstrong, Denison, Tx. 75020. Check, Money Order, VISA or Master Charge accepted. Phone orders (charge only) call (214) 465-7805. Freight prepaid. Allow 3 weeks for personal checks to clear. Texas residents add 5%. Foreign orders add 30%. Prices subject to change without notice. COD's not accepted.