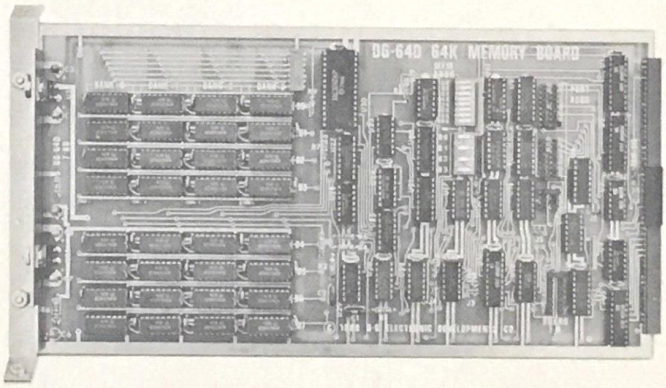
ERIC MACH
703-6110

OPERATION MANUAL

DG-64D
DG-64D5
64K RAM



Please read Operator's Manual prior to installing or operating this device. Your warranty may be affected by failure to read the Operator's Manual prior to installation.

D·G ELECTRONIC DEVELOPMENTS CO.

(214) 465-7805
P.O. Box 1124, 1827 South Armstrong
Denison, Texas 75020

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SPECIFICATIONS

ORGANIZATION	64K Bytes Hardware Selectable in 8K Byte Blocks Software Selectable in 16K Byte Blocks (Hardware deselect overrides software select)		
ADDRESS SELECTION	Hardware — Dipswitch Software — I/O Port		
ACCESS TIME	240 ns (Typical)		
INTERFACE	Heath® H8 Bus Compatible. All inputs 1 TTL load or less.		
I/O PORT SELECTION	Any of the 256 available I/O Ports selected by solderless jumper.		
REFRESH	On-board 8080A or Z80A compatible refresh backed up by asynchronous refresh — Also operates with DG-80 Z80 type refresh.		
SOCKETS	All I.C.'s socketed		
POWER REQUIREMENTS (Typical) (2MHz)	DG-64D	+ 14▸20 VDC @ 120 mA + 7▸14 VDC @ 400 mA − 14▸20 VDC @ 20 mA	
	DG-64D5	+ 7▸14 VDC @ 500 mA	
(4MHz)	DG-64D	+ 14▸20 VDC @ 185 mA + 7▸14 VDC @ 415 mA − 14▸20 VDC @ 20 mA	
	DG-64D5	+ 7▸14 VDC @ 560 mA	
MEMORY DEVICES	DG-64D	4116	(or equivalent)
	DG-64D5	4517	(or equivalent)

D-G Electronic Developments Company reserves the right to discontinue products and to change specifications at any time without incurring any obligations to incorporate new features in products previously sold.

Heath and H8 are registered trademarks of the Heath Company, Benton Harbor, Michigan. Z80 is the registered trademark of Zilog Corporation. CP/M is the registered trademark of Digital Research Corp., of Pacific Grove, California.

INTRODUCTION

The DG Electronic Developments Company Model DG-64D is a 64K by 8 bit memory board designed for use with the Heath® H8 computer. The board is designed to be fully compatible with all present Heath® H8 peripherals and memory as well as all H8 Bus products provided by DG Electronic Developments Company. Features of the DG-64D include:

- Up to 64K byte capacity
- Hardware bank selectable in 8K byte increments
- Software bank selectable in 16K byte increments through I/O port
- On-board bank select/CPU ROM disable port addressable to any of 256 I/O addresses
- Up to eight boards controllable through one I/O port allowing 'page mode' operation
- On-board transparent refresh for 8080 or Z80 microprocessor backed up by asynchronous refresh upon loss of normal program execution
- Low power consumption — less than 8 watts
- Fully factory assembled and tested

The DG-64D5 memory board provides all of the above features as well as offers single 5-volt supply operation. This allows for flexibility in the use of peripheral devices.

OPERATION

HARDWARE BANK SELECTION

The 64K byte memory space of the DG-64D is divided into 8 hardware selectable 8K byte blocks as shown in Fig. 1. These blocks may be selected by the MEM ADDR switch, S2 (see Fig. 2) and are identified on the board by the starting address of each block. For example, the block of memory occupying the address space from ØK up to 8K is labeled ØK on the MEM ADDR switch; the block of memory from 8K to 16K is labeled 8K on the MEM ADDR switch, etc. Note that blocks of memory deselected by the MEM ADDR switch **cannot** be enabled through the software bank select port described below.

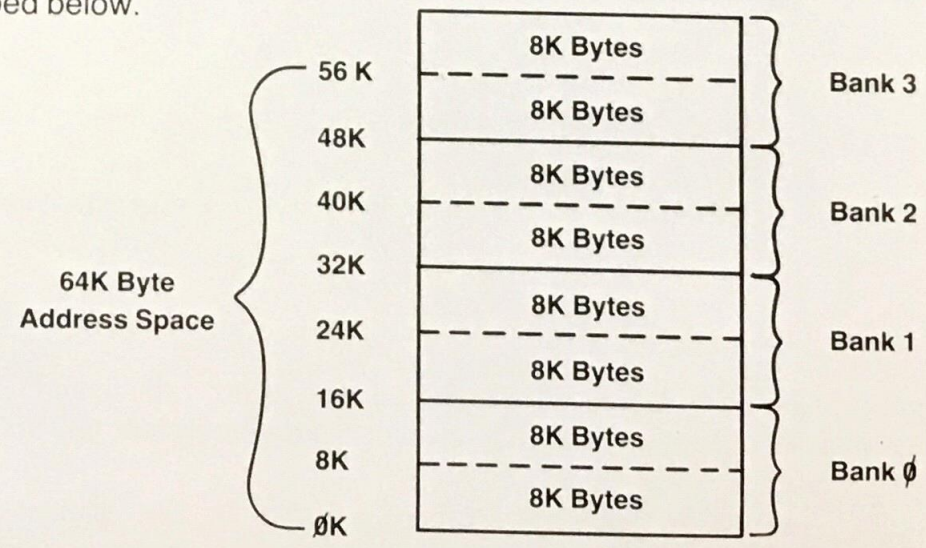


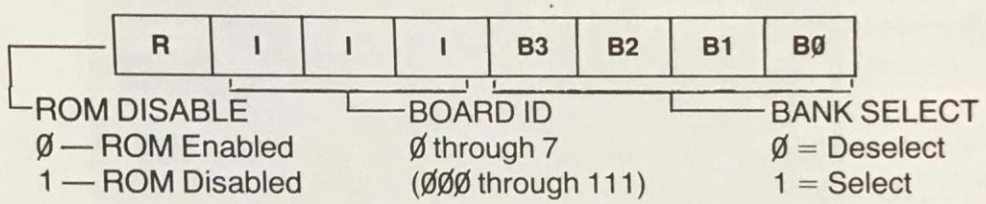
Figure 1: DG-64D Memory Organization

SOFTWARE BANK SELECTION

The DG-64D memory board is organized as four 16K byte software selectable banks. These banks occupy the memory space in the following manner:

BANK Ø	ØK through 16K
BANK 1	16K through 32K
BANK 2	32K through 48K
BANK 3	48K through 64K

Upon power-up or MASTER CLEAR, the active banks are determined by the 'power-on bank enable switch' S1 (see Fig. 2). After the system is running, the status (select or deselect) of the four banks as well as the status of 'ROM DISABLE' (CPU memory disable) is determined by the word contained in the Bank Select/ROM Disable control port on the DG-64D. This 8-bit control word has the following format:



The bank select bits of the control word will simply be 1's if the specified bank is to be selected or Ø's if the bank is to be deselected. The 'BOARD ID' will be the 3-bit binary equivalent of the decimal Board ID number (i.e. ØØØ for Board Ø, ØØ1 for Board 1, Ø1Ø for Board 2, etc.). The 'ROM DISABLE' bit will be a Ø if the CPU memory is to be enabled and a 1 if this memory is to be disabled.

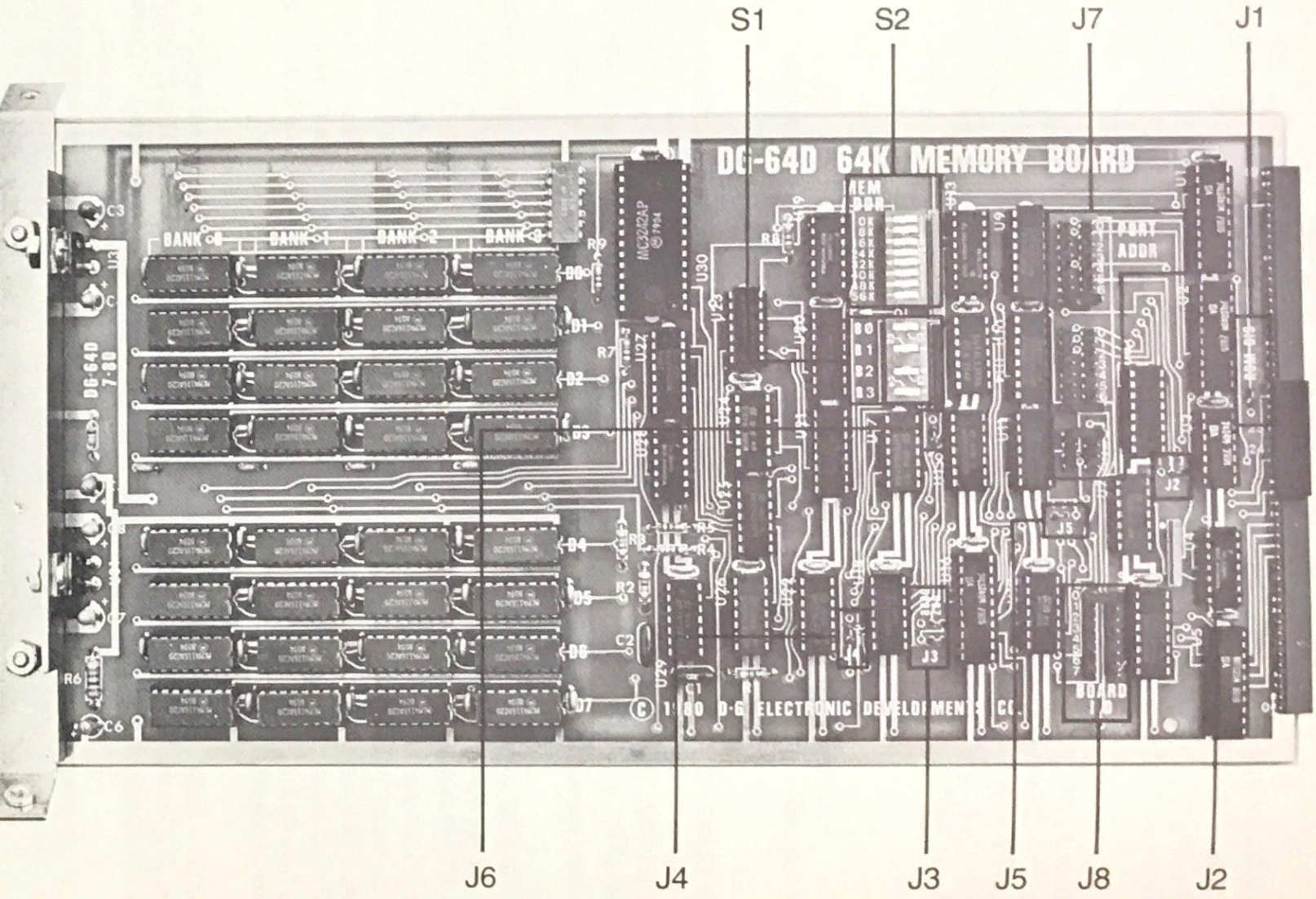
NOTE: Upon power-up or MASTER CLEAR, the CPU memory will always be enabled!

The control word may be written to the control port at any time a change in the Bank Select/ROM Disable status is desired although care must be exercised so that a required portion of memory such as the stack area or soon-to-be accessed program memory is not disabled.

If it is desired to use more than one DG-64D in the computer, all boards should utilize the same I/O port but be assigned individual board ID's. When the system is configured in this manner, enabling a specific bank on one board will automatically disable the corresponding bank on all other DG-64D's addressed at that I/O port. This protection feature prevents bus contention among memory boards that could damage data bus drivers. When a specific bank on a board is disabled, the status of the corresponding bank on the remaining boards is not affected.

WARNING: If more than one DG-64D is installed in the computer, the Power-on Bank Enable switches (S1) on the boards should be set such that a given bank (Ø through 4) is enabled on **only one** board upon power-up. This will prevent bus-contention when the system is first powered up.

As mentioned previously, if a block of memory is deselected through the MEM ADDR switch, this block cannot be re-enabled using the software bank select port. For example, if the ØK block were turned off on the MEM ADDR switch, then selecting BANK Ø through software would only enable the 8K byte block from 8K through 16K.


S1
S2
J7
J1
DG-64D 64K MEMORY BOARD
BANK 0
BANK 1
BANK 2
BANK 3
J6
J4
J3
J5
J8
J2

The functions of each of the switches and jumpers in Figure 2 are described below:

S1 — Power-on Bank Enable — The DG-64D 64K byte memory space is divided into four 16K byte blocks (Bank Ø through Bank 3) for software selection. This switch determines which banks (if any) are active upon power-up or MASTER CLEAR of the H8 system. These bank selections may be over-ridden by software bank selection. The "ON" position will have the switches depressed toward the labels BØ through B3.

S2 — MEM ADDR — This switch enables the 64K byte RAM space in 8K byte increments, labelled by the starting address of each block. Deselection of a block by this switch cannot be over-ridden by software bank selection. The "ON" position will have the switches depressed toward the labels ØK through 56K.

J1 — ROM Disable Jumper — This jumper should be connected from the center hole to the 'ROM DIS' position if the ROM disable (CPU Memory Disable) function is desired. If the ROM disable function is not desired, no jumper should be installed.

J2 — RFSH Polarity — This jumper determines whether external refresh signals will be interpreted as active "high" or active "low". This jumper should be set from "2" to "3" for use with the DG-80 Z80 CPU.

J3 — 8080 or Z80 — This jumper determines proper timing for asynchronous refresh when using the 8080 or Z80 microprocessor. For the Z80, both jumpers should be in the right hand (Z80) positions. For the 8080, the lower jumper should be in the right hand position and the upper jumper should be in the left hand (8080) position.

J4 — Delay — This jumper is used to insert delay on memory access cycles when using the 8080 CPU with the 8238 System Controller (as in the Heath® 8080 CPU). The jumper should be connected from "1" to "2" if the Heath® CPU is used. If the DG-80 Z80 CPU is being used, the jumper should be connected from "2" to "3".

J5 — Refresh Mode — This jumper determines whether the DG-64D on-board refresh is active or external refresh signals are used. For on-board refresh (recommended mode), the jumper should connect "1" to "2". For external 'Z80 type' refresh, the jumper should connect "2" to "3".

J6 — Asynchronous Refresh Rate — The asynchronous refresh rate of the DG-64D is designed to be once every 13 microseconds to maintain memory contents yet minimize power dissipation. This jumper allows the 13 microsecond refresh rate to be maintained for operation at 2 or 4 MHz clock frequencies. Therefore this jumper should be connected in the position appropriate for your CPU clock frequency.

J7 — PORT ADDR — This set of jumpers determines the address of the I/O port used for bank selection and ROM disable. The top jumper is the low-order digit, the middle jumper is the middle digit and the bottom jumper is the high order digit of the **OCTAL** I/O port address.

J8 — Board ID — When more than one DG-64D board is used in the system, each board is assigned a 'Board ID' number from Ø to 7. This allows for the protection features described previously. If only one board is in use, Board ID Ø is recommended for that board.

SYSTEM EXAMPLES

The following system examples are given to illustrate the use of the DG-64D. Refer to Figure 1 for location of the switches and jumpers.

EXAMPLE 1: System consists of Heath® 8080 CPU, DG-64D and will be operated with H17 disk system utilizing 56K RAM:

SWITCH OR JUMPER	SETTING
S1	All switches "ON"
S2	ØK "OFF" (open) All others "ON"
J7	Ø77
J1	No Jumper
J2	2 to 3
J3	Lower Jumper Z80, Upper Jumper 8080
J4	1 to 2
J5	1 to 2
J6	2 MHz
J8	Ø

EXAMPLE 2: System consists of DG-80, Z80 CPU (2 MHz), DG FP8 Monitor package, DG-64D, require 64K RAM for CP/M®.

SWITCH OR JUMPER	SETTING
S1	B3 "OFF", all others "ON"
S2	All switches "ON"
J7	Ø77
J1	ROM "DIS"
J2	2 to 3
J3	Upper **and** Lower Z80
J4	2 to 3
J5	1 to 2
J6	2 MHz
J8	Ø

The DG-80 MEM ADDR switch should be set to locate the CPU on-board memory at 48K. Upon power-up, the FP-8 firmware will transfer ROM information into low RAM and then enable bank B3 so that the full 64K RAM space may be utilized. NOTE: If this system were to be operated at 4 MHz, then J6 would be set to 4 MHz.

EXAMPLE 3: System consists of DG-80, Z80 CPU (2 MHz), DG FP8 Monitor package, 1 DG-64D (fully populated), 1 DG-64D (Banks 1, 2 and 3 populated — i.e., 48K beginning at 16K) — top 48K of RAM to be bank selected.

The fully populated board would be set as follows:

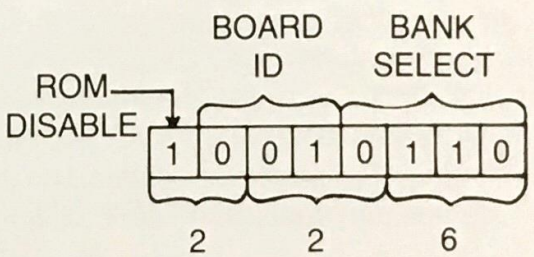
SWITCH OR JUMPER	SETTING	SWITCH OR JUMPER	SETTING
S1	B3 "OFF", all others "ON"	J3	Upper **and** Lower Z80
S2	All switches "ON"	J4	2 to 3
J7	Ø77	J5	1 to 2
J1	ROM "DIS"	J6	2 MHz
J2	2 to 3	J8	**ø**

The partially populated board would be set:

S1	All Banks "OFF"	J3	Upper **and** Lower Z80
S2	ØK, 8K "OFF", all others "ON"	J4	2 to 3
J7	Ø77	J5	1 to 2
J1	Does not matter	J6	2 MHz
J2	2 to 3	J8	**1**

Note that both boards must use Port Ø77 for the control port in order to preserve the protection features described in the Software Bank Selection section of this manual. The DG-80 MEM ADDR switch should be set to locate the CPU on-board memory at 48K. Upon power-up, the FP-8 firmware will transfer ROM monitor information into low RAM of Board Ø (the fully populated board) and then enable bank B3 so that the full 64K RAM space of Board Ø may be utilized. Board 1 (the partially populated board) will not be accessible until the proper control word is written to the bank select control port.

The only limitation to utilizing the memory available on Board 1 is that necessary program memory or stack space must be preserved. Since the FPM/80 monitor utilizes space at the bottom of RAM (Bank Ø) and stack area at the top (Bank 3) special care must be taken if these banks are assigned to Board 1. Banks 2 and 3 may be assigned to Board 1 by writing the following control word to Port Ø77:



Octal Control Word

The effect of this control word may be interpreted as follows (refer to the Software Bank Select section of this manual for bit identification):

The "ROM DISABLE " bit is a "1" so that the CPU on-board memory will continue to be disabled.

The three bit "Board ID" is ØØ1 since we want to change the status of Board 1.

The Bank Select bits representing banks 1 and 2 are set to "1" to turn on these banks on Board 1. This will automatically turn off banks 1 and 2 of Board Ø.

Since the bits representing banks Ø and 3 are set to Ø these banks will remain assigned to Board Ø.

The 64K byte memory space of the computer will still be continuous and accessible; however, when data is written to or read from banks 1 and 2, the data will be on Board 1. Data in banks 1 and 2 of Board Ø will be unaffected by these accesses. If one wishes to return to the data in banks 1 and 2 of Board Ø, the control word written to Port Ø77 would be 217. All memory in the 64K memory space would then be accessed from Board Ø.

If the user wishes to utilize Bank 3 of Board 1, he must first insure that the FPM/80 stack area is preserved. This may be accomplished by first disabling the interrupts (this prevents the panel monitor from attempting to use the stack while it is being transferred) and then transferring the whole stack (64 bytes) to an area of memory which will not be disturbed. Bank 3 (as well as other banks) may now be assigned to the desired board(s) and the stack transferred to its normal location at the top of Bank 3. The interrupts may then be re-enabled and system operation resumed.

WARNING: THE ABOVE DISCUSSION ASSUMES THE USE OF THE FPM/80 PANEL MONITOR ONLY. VARIOUS OPERATING SYSTEMS AND APPLICATIONS SOFTWARE WILL REQUIRE PRESERVATION OF OTHER MEMORY SPACE. THE USER SHOULD REFER TO THE USERS' MANUAL SUPPLIED WITH HIS PARTICULAR SOFTWARE TO DETERMINE THESE AREAS.

Note: When multiple DG-64D memory boards are used in a single mainframe, care should be exercised so that the power supply current capability of the computer is not exceeded. The critical power supply that should be checked is the +14▸20 V. supply of the Heath H8. The current requirement for this supply is given in the Specifications section of this manual and refers to a single DG-64D in the computer. The typical current requirement for **each additional** DG-64D is 75 mA at a clock frequency of 2 MHz and 100 mA at a clock frequency of 4 MHz. The total +14▸20 V. supply current of **all** boards (CPU, Serial Interfaces, etc.) in the computer should be determined and this value **should not exceed 500 mA** for safe operation.

INSTALLATION

To install your DG-64D in the H8 computer, perform the following steps:

Ø Disconnect your H8 from the power outlet.

1 Remove the top cover and tie bracket of your H8 computer.

2 Set the DIP switches and jumpers on the DG-64D for your desired system configuration using the information presented in the DG-64D "OPERATION" section of this manual.

3 Place the DG-64D inside the H8 mainframe and carefully push the end connectors onto the desired plugs on the mother board. Be sure the pins are aligned properly with the end connectors.

4 Install a screw through the chassis bottom into the DG-64D heat sink bracket.

5 Reinstall the tie bracket and top cover on the computer.

6 Turn on the computer. The **PWR, RUN, MON,** and **ION** LED's should light and the display should be random numbers.

If the DG-64D fails to function properly at this point, review the DG-64D "OPERATION" section of this manual and then repeat the above installation procedure.

UTILIZING THE DG-64D WITH OTHER MEMORY BOARDS

The fully populated DG-64D memory board provides full H8 memory capacity on a single PC card, however, some users may wish to utilize a partially populated DG-64D in conjunction with other available memory. The user should first refer to the system memory map of Figure 1 in this manual to determine which portions of the memory space are to be occupied by the DG-64D and which portions are to be occupied by other memory boards. Jumpers and or switches may then be set on all memory boards to address them to the appropriate portions of the memory space.

NOTE: In order for a bank of memory (or a portion of a bank) to be used, RAMs **must** be installed in that bank. Since partially populated DG-64D's are always shipped with Bank Ø populated, the user may find it necessary to remove these memory devices and relocate them to another bank for maximum utilization of available memory. Care should be exercised when performing this relocation as the devices are static sensitive and may be damaged by improper handling. Refer to the Memory Expansion section of this manual for RAM installation procedures.

MEMORY EXPANSION

The DG-64D DG-64D5 may be purchased with no RAM installed or with RAM installed in 16K increments up to a maximum of 64K. If the board was purchased with less than 64K RAM, additional 16K "Chip Sets" (8 memory devices) may be purchased from DG Electronic Developments Company as well as other vendors.

NOTE. If memory chip sets are purchased from a vendor other than DG, you should specify 4116-type RAMs for the DG-64D and 4517-type **single supply** RAMs for the DG-64D5. These RAMs

must have an access time of 200 ns or less in order to meet the full specifications of the DG-64D/DG-64D5.

Memory chip sets may be installed as follows:

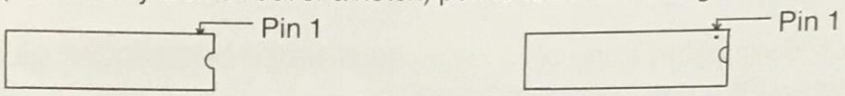
Ø) Remove your DG-64D/DG-64D5 from the H8 computer.

1) Locate the bank you wish to populate. The board should always be populated as one complete bank at a time — partially populated banks will not operate properly.

2) Make sure that memory devices you have are the proper type for the board version (DG-64D or DG-64D5) you have.

   WARNING: DO NOT ATTEMPT TO MIX 4116-TYPE DEVICES AND 4517-TYPE DEVICES ON ONE MEMORY BOARD. THE DG-64D WILL ONLY OPERATE WITH 4116-TYPE DEVICES AND THE DG-64D5 WITH 4517-TYPE DEVICES. DAMAGE MAY OCCUR TO THE RAM DEVICES OF THE DG-64D/DG-64D5 IF THE WRONG MEMORY DEVICES ARE USED.

3) Install the 8 memory devices in the desired bank. Be sure that the pin 1 end of the memories (denoted by a small dot or a notch) points **toward** the edge connector of the memory board.



4) Re-install the DG-64D/DG-64D5 in the computer and use the Heath H17 memory test (or equivalent) to check for proper operation.

TIMING DIAGRAMS AND SCHEMATIC

The following timing diagrams and schematics are included for the use of persons wishing to repair or modify their board after the warranty period has lapsed. (Remember, any attempt to modify or repair the board during the warranty period will void the warranty!)

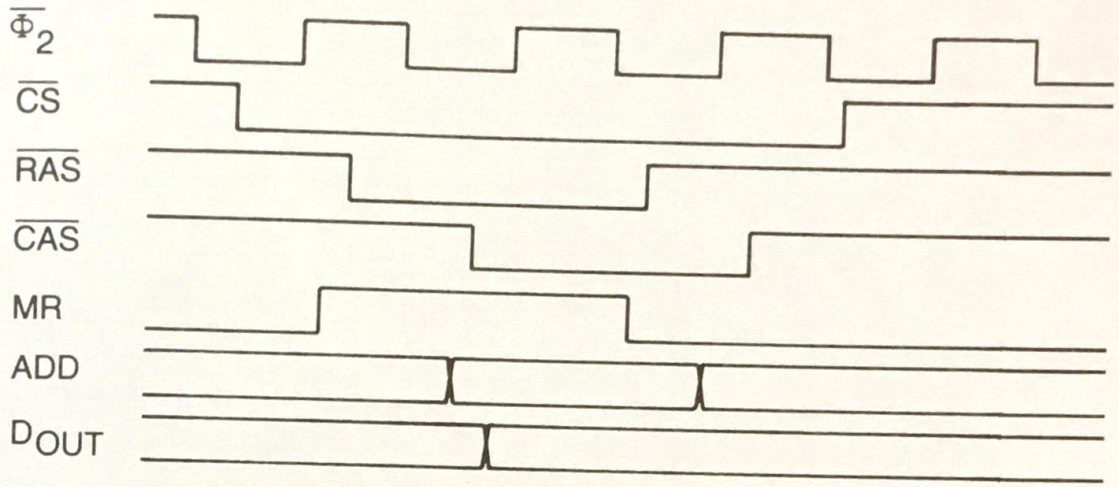
The signals displayed on the timing diagrams were viewed at the following places:

$\overline{CS}_{B\emptyset}$	U27	Pin 2	$\overline{CAS}$	U29	Pin 8
$\overline{CS}_{B1}$	U27	Pin 14	MR	U7	Pin 12
$\overline{CS}_{B3}$	U27	Pin 5	MW	U7	Pin 1Ø
$\overline{CS}_{B4}$	U27	Pin 11	$\overline{W}$	U29	Pin 11
$\overline{RAS}_{B\emptyset}$	U27	Pin 4	M1	U3	Pin 9
$\overline{RAS}_{B1}$	U27	Pin 12	$\overline{REF\ EN}$	U3Ø	Pin 2
$\overline{RAS}_{B2}$	U27	Pin 7	Φ_2	U3	Pin 11
$\overline{RAS}_{B3}$	U27	Pin 9			

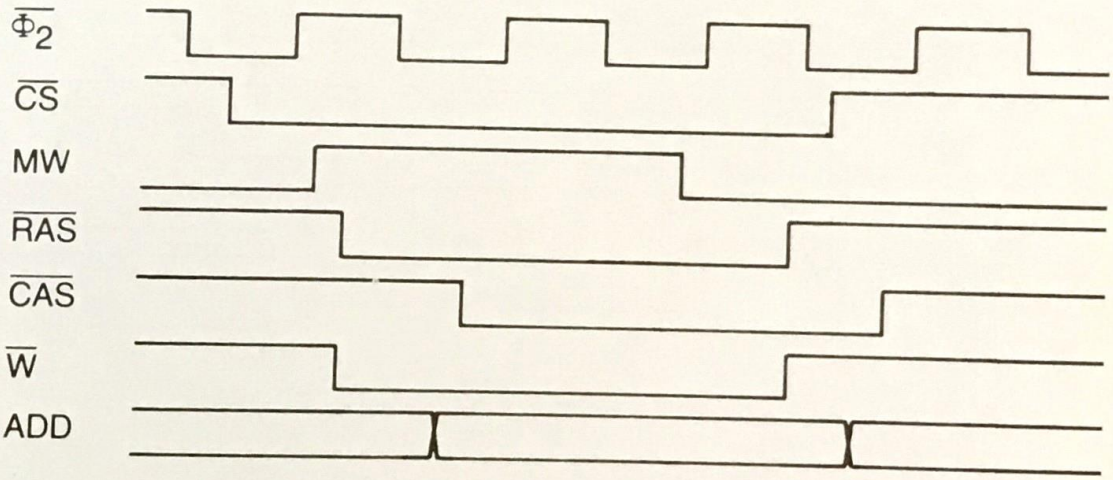
TIMING DIAGRAMS

These timing diagrams apply to the DG-64D operating in a system using the Heath® 8080A CPU with the 8238 type system controller.

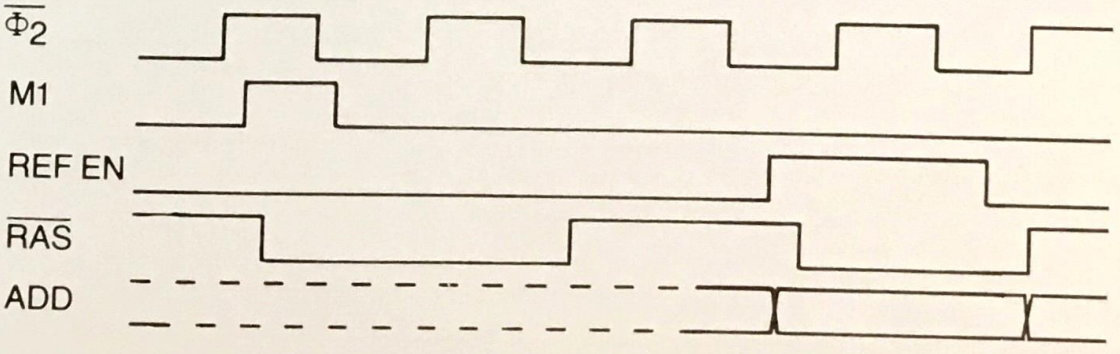
MEMORY READ



MEMORY WRITE

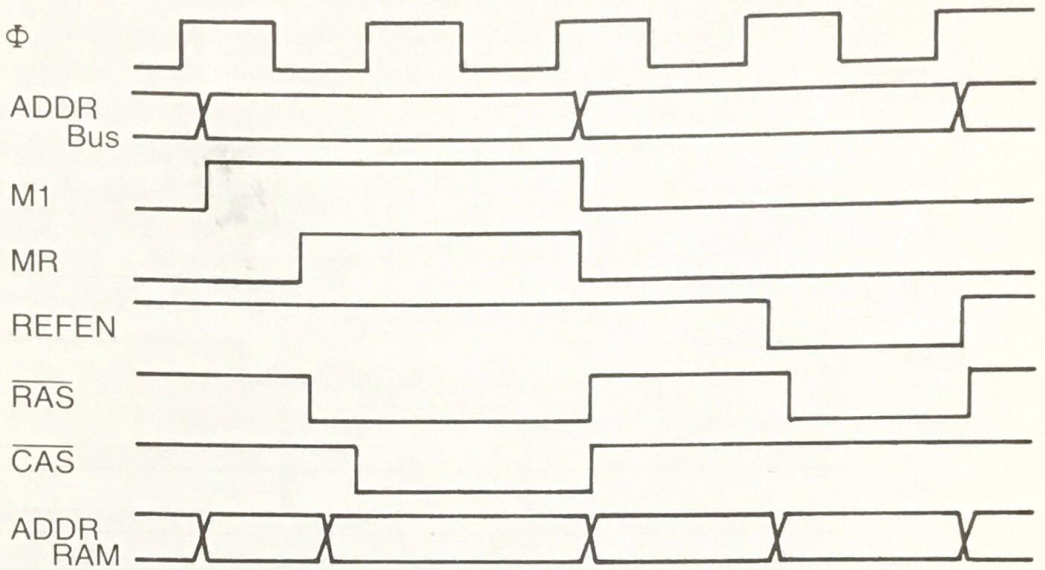


REFRESH

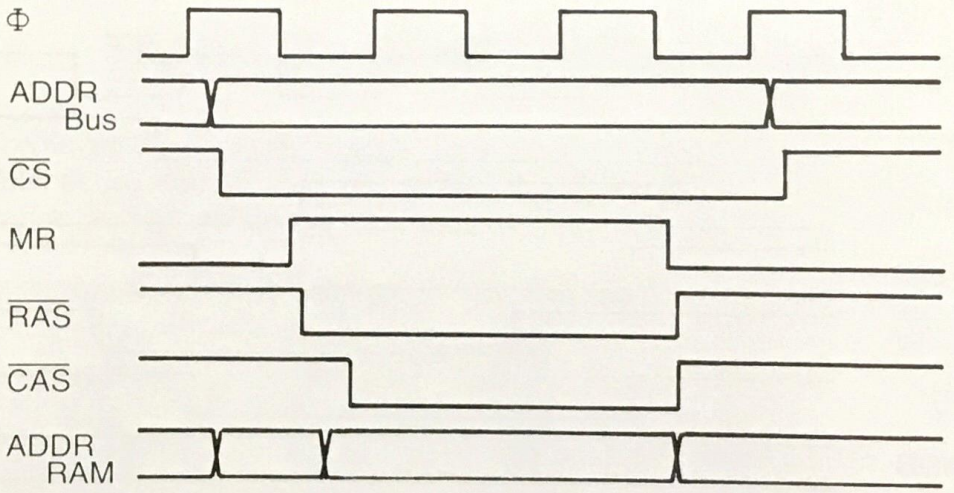


These timing diagrams apply to the DG-64D in a system using the DG-80 CPU.

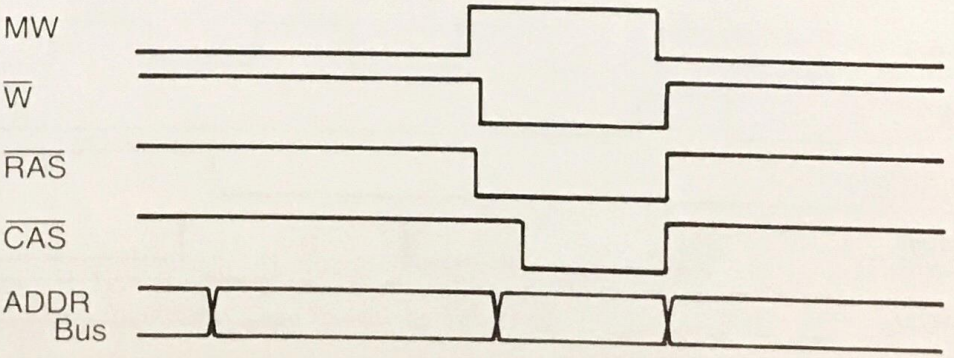
INSTRUCTION FETCH (INCLUDING ONBOARD REFRESH)



MEMORY READ



MEMORY WRITE



DG-64D / DG-64D5 64K RAM BOARD

LIMITED WARRANTY

The DG-64D is warranted for a period of ninety (90) days from the date of purchase to be free from defects in material and workmanship. Should this product fail to perform satisfactorily, arrangements should be made with D-G Electronic Developments Co. for warranty service as follows.

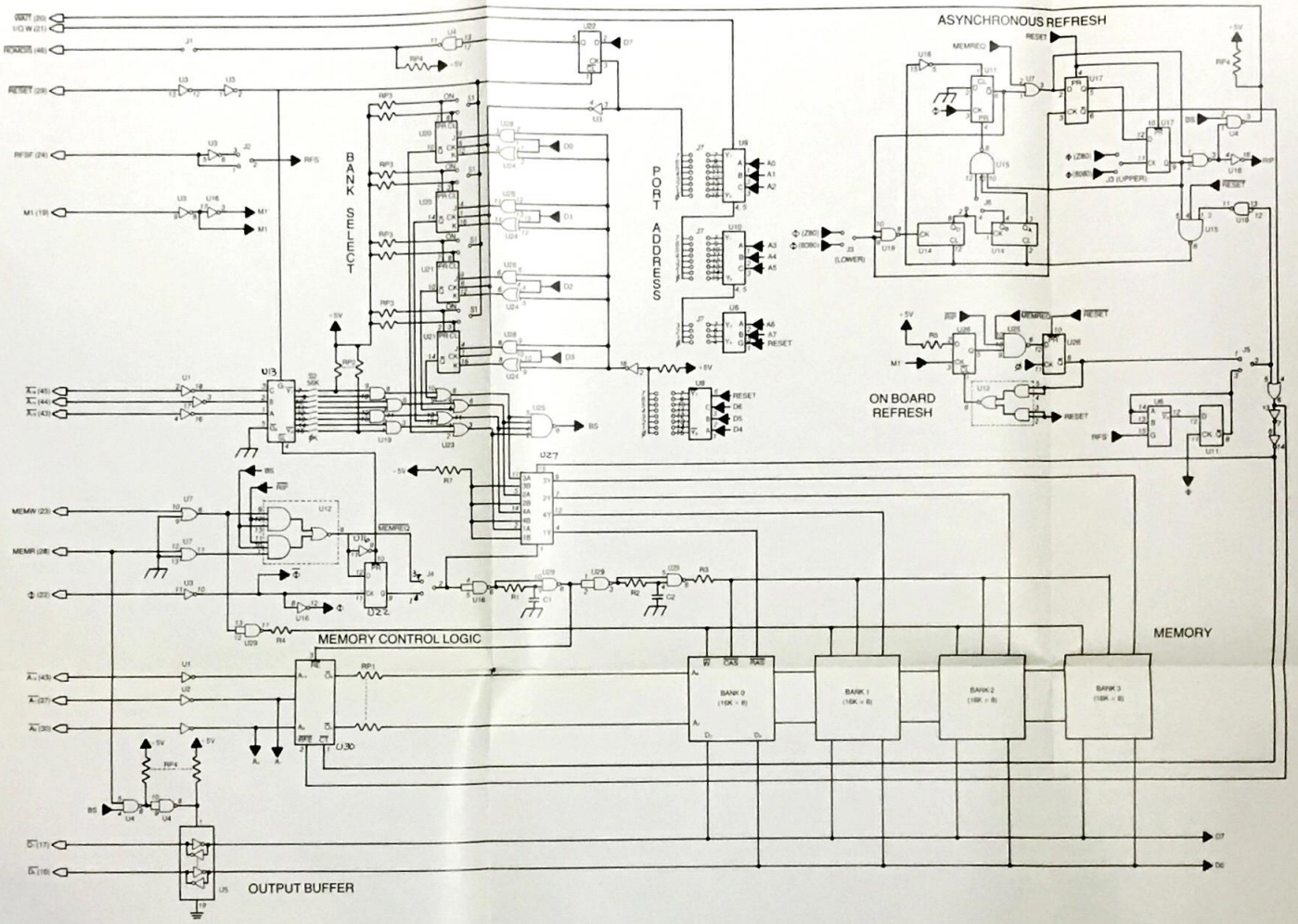
Return of the DG-64D is subject to the issuance of a RETURN MERCHANDISE AUTHORIZATION NUMBER by D-G Electronic Developments Co. This RMA number must be clearly visible on the outside of the returned package which must be returned freight pre-paid. FAILURE TO CONFORM WITH THIS PROCEDURE WILL RESULT IN REFUSAL TO ACCEPT SAID PACKAGE UPON ARRIVAL.

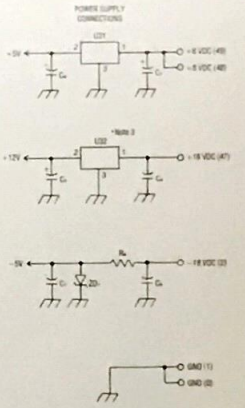
D-G Electronic Developments will, at our option, repair or replace defective units received during the warranty period. This warranty is invalid if the product has been misused or modified. Warranty is limited to replacement of defective parts and no responsibility is assumed for damage to other equipment.

This warranty is made in lieu of all other warranties expressed or implied and is applicable only to the product as shipped from the factory.

NOTICE:

REMOVAL OR ALTERATION OF THE IDENTIFICATION TAG ON THE REVERSE SIDE OF THE DG-64D MEMORY BOARD WILL VOID THE ABOVE WARRANTY.





DG-64D ©1985
DG ELECTRONIC DEVELOPMENTS CO
DENISON, TEXAS 75020
4-85

PARTS LIST

MEMORY DEVICES	4116 (300ns)
U1, U2, U16	74LS240
U3	74LS04
U4	74LS32
U5	74LS645 (ST 125)
U6	74LS139
U7, U23	74LS32
U8, U9, U10	74LS138
U11, U17, U22, U28	74LS74
U12	74LS51
U13	74LS157
U14	74LS393
U15, U25	74LS20
U18, U29	74132
U19, U26	74LS08
U20, U21	74LS76
U24	74LS86
U27	74107
U30	3242
U31	LM340T-5
U32	LM340T-12 (LM340T-5 for DG-64/3s)
R1	1 K ohm, ¼w
R2	1 K ohm, ¼w
R3, R4	33 ohm, ¼w
R5, R7, R8, R9	1 K ohm, ¼w
R6	1 K ohm, ¼w
C1	82 pf, Silver Mica
C2	82 pf, Silver Mica
C3	10mf, 25v Tantalum
C4, C7, C8	10mf, 16v Tantalum
C5, C6	2.2mf, 25v Tantalum
ZD1	1N5231, 5.1v Zener Diode
RP1	33 ohm DIP Resistor
RP2	1 K ohm, 10 pin SIP Resistor
RP3	1 K ohm, 4 pin SIP Resistor
RP4	1 K ohm, 8 pin SIP Resistor

DG-64D NOTES

1. ( ) DENOTES PIN NUMBERS ON HEATH® H8 BUS.

2. POWER SUPPLY PIN CONNECTIONS ARE AS FOLLOWS:

COMPONENT(S)	GROUND	+5V	+12V	-5V
74LS240, 74LS640, 74LS04, 74LS08,	10	20	–	–
74LS74, 74LS51, 74LS393, 74LS20,	10	20	–	–
74132, 74LS08, 74LS86, 74LS107	7	14	–	–
74LS138, 74LS139	7	14	–	–
74157	8	16	–	–
74LS76	13	5	–	–
MC3242	14	28	–	–
4116 (DG-64D)	16	9	8	1
4517 (DG-64D5)	16	8	–	–

3. THE FOLLOWING COMPONENTS ARE NOT PRESENT ON THE DG-64D5: C5, C6, R6, ZD1. U32 IS A LM340T-12 FOR THE DG-64D AND A LM340T-5 FOR THE DG-64D5.

4. THE FOLLOWING SIGNAL LINES WERE NOT MARKED ON THE SCHEMATIC IN THE INTEREST OF SPACE:

DATA BUS BUFFER: U5

BUS INPUTS	PIN	BUFFER OUTPUTS	PIN
D0	11	D0	9
D1	12	D1	8
D2	13	D2	7
D3	14	D3	6
D4	15	D4	5
D5	16	D5	4
D6	17	D6	3
D7	18	D7	2

ADDRESS BUFFERS A0 THROUGH A7: U2

BUS INPUT	PIN	BUFFER OUTPUT	PIN
A0	11	A0	9
A1	8	A1	12
A2	13	A2	7
A3	6	A3	14
A4	15	A4	5
A5	4	A5	16
A6	17	A6	3
A7	2	A7	18

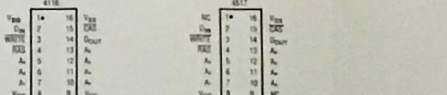
A8 THROUGH A15: U1

BUS INPUT	PIN	BUFFER OUTPUT	PIN
A8	11	A8	9
A9	8	A9	12
A10	13	A10	7
A11	6	A11	14
A12	15	A12	5
A13	4	A13	16
A14	17	A14	3
A15	2	A15	18

5. THE FOLLOWING UNUSED TTL DEVICE INPUTS ARE "PULLED-UP" TO +5V:

INPUTS	PULL-UP
U26-pin 2, 4, 13	R5
U22-pin 4, 13	R5
U17-pin 1, 13	R5
U11-pin 13, 10	RP-2

6. PIN-OUTS FOR THE MEMORY DEVICES USED ARE AS FOLLOWS:



WARNING: DO NOT ATTEMPT TO MIX 4116 DEVICES AND 4517 DEVICES ON THE SAME BOARD AS THE POWER SUPPLY REQUIREMENTS FOR THESE COMPONENTS ARE NOT THE SAME.

7. PIN-OUT OF THE MC3242 (U30) IS AS FOLLOWS: